

RTD2871FA

4K2K Smart TV Controller

Specification

Version 0.8

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek RTD2996S series chip.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

1 Introduction

RTD2871 is 4K Smart TV SoC enhanced from previous successful RTD2991 Controller. RTD2871 contains quad core CPUs, powerful 3D GPU, video decoder, de-interlacer, scaler, color engine, evariant inputs for video signals , embedded demod and etc. The universal demod is embedded to supports DTMB / ATSC / DVB-C / DVB-T / DVB-S / ISDB-T / **DVB-T2 / DVB-S2 / S2X** DTV . The embedded 3D GPU is capable of 4K2K OSD drawing. The system CPU is ARM 64 bit CPU quad core with 1024KB L2 cache. The voltage for CPU can be adjusted for boosting performance or power saving by using external PMU. **RTD2871 integrates a higher grade FRC to convert to 4K60fps output with very smooth de-judder performance. Multiple TCON-less spec supported includes EPI , CEDS , and CMPI .** RTD2871 is capable of decoding 4K2K HEVC/VP9 60Hz. **The latest HDR decoder technologies are built-in , including Dolby Vision HDR , UHD-A (SMPTE) HDR10 , Technicolor HDR , HLG (Hybrid Log Gamma) .**

- Brief chip information :
 - Power supply : 1.0V(CPU)/1.0V(Core) / 1.5V(DDR3)/ 3.3V
- Brief external BOM and system information :
 - DDR usage :
 - ◆ Built in DDR and external supported.
 - Package :
 - ◆ EDHS-PBGA 27x27
 - XTAL : 27MHz
 - **eMMC 5.1 compatible HS400**
 - Serial FLASH : support up to 64Mbytes
 - Panel SPEC :
 - ◆ **4K@60Hz via 8 lanes Vby1**
 - ◆ **4K@60Hz via 12 lanes EPI**
 - ◆ **4K@60Hz via 12 lanes CEDS**
 - ◆ **FHD@120hz via Vby1**



- RTD2871 adopts ARM Processor .
- Dolby Audio , Dolby Vision words , logo , trademark are owned by Dolby Company
- Technicolor words , logo , trademark are owned by Technicolor Company

2 Feature List

- Audio Input/Output
 - ◆ 4 pairs Analog Stereo Line level inputs
 - ◆ 3 pairs for Audio Stereo Line Output.
 - ◆ Headphone Amplifier embedded
 - ◆ 48KHz baseband ADC Sample rate
 - ◆ 48KHz Audio Sample rate on TV Sound De-modulator
 - ◆ Four Digital I2S slave/master input and Three Digital I2S Output.
 - ◆ Support individual SPDIF out & ARC(SPDIF) out
 - ◆ SPDIF/ARC out support both PCM & Non-PCM format
- Video Input
 - ◆ **4 Channel** HDMI 1.4/2.0 compliant receiver w/ one MHL 2.0/3.0
 - ◆ Support HDMI 2.0 3D mandatory format and 4K2K format input
 - ◆ Integrated HDCP 2.2 decryption engine for receiving protected audio and video content
 - ◆ Pre-programmed HDCP keys provide highest level of key security, simplifies manufacturing
 - ◆ Support HDMI CEC interface
- Video Decoder
 - ◆ Line-Locked clock generation.
 - ◆ Horizontal and vertical sync detection and locking.
 - ◆ H/W auto multi-standard detection and color decoding:
 - ◆ Support NTSC/PAL/SECAM decode
 - NTSC-M, NTSC-443.
 - PAL-BDGI, PAL-M, PAL-N, PAL-60, PAL-CN
 - SECAM.
 - ◆ High performance adaptive 3D comb filter for Y/C separator.
- Audio Decoder
 - ◆ Supports multi-standard TV broadcasting includes BTSC, EIA-J and FM A2.
 - ◆ NICAM sound for B/G/L/I/D/K system.
 - ◆ Automatic Standard Sound Detection
- VBI Decoder
 - ◆ CC : CC1, 2, 3 and 4, Text 1, 2, 3 and 4, XDS (eXtension Data Service), V Chip
 - ◆ CGMS : ETSI EN 300 294, ITU-R BT.119 method, IEC-61880 method, CC-XDS method
 - ◆ WSS : ETSI EN 300 294, ITU-R BT.119 method, IEC-61880 method, CC-XDS method
 - ◆ TT: Teletext 1.5/2.5 ETSI EN 300 706

- **ATV IF Demodulation**
 - ◆ Fully Support NTSC, PAL, SECAM IF Demodulation.
 - ◆ Multistandard true synchronous demodulation with active carrier regeneration.
 - ◆ Normal IF and Low IF supported
 - ◆ VIF AGC detector for gain control.
 - ◆ SIF-AGC for gain controlled SIF amplifier, Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode, PLL controlled.
 - ◆ SAWless
- **DTV demod**
 - ◆ Embedded DTMB / ATSC / DVB-C / DVB-T / DVB-S / ISDB-T / **DVB-T2 / DVB-S2 / S2X** Demod
- **Multi-format Video Codec**
 - ◆ Support MPEG1/2 and VC-1,AVS, AVS+, MPEG4, RM/RMVB up to full HD (1920x1080)
 - ◆ H.264 1080p encoder
 - ◆ H.264 4K2K@60Hz decoder
 - ◆ HEVC 10bits 4K2K@60Hz decoder
 - ◆ VP9 **10 bits** 4K2K@60Hz decoder
 - ◆ **SHVC 10 bits 4K2K@60Hz decoder**
- **Video Post-Processing**
 - ◆ Automatic Video Error Concealment
 - ◆ MPEG De-block & De-ringing noise reduction filter
- **Audio Decompression**
 - ◆ Support AC3, MPEG1 Layer 1,2 and 3(mp3), AAC, DTS, and MPEG2 Layer 2, audio format decoding
 - ◆ Support audio transcoding
 - ◆ **Support Dolby Audio MS11 / MS12**
 - ◆ **Support Dolby Audio AC-4**
 - ◆ **Support Dolby ATMOS**
- **Audio Post-Processing**
 - ◆ Hardwired Automatic Volume Control, 11-stage Equalizer, Treble/Bass/Loudness/Volume/ Balance control
 - ◆ RealStereo, RealSurround, RealSpace, RealVoice, RealEnvironment, Dynamic Speaker
- **Image Processor**
 - ◆ Input format detection and Smart-Fit™
 - ◆ Compatibility with standard VESA mode and support user-defined mode
 - ◆ Frame-Lock display to keep smooth motion
 - ◆ Color-Recover™III for video cross color reduction
 - ◆ Clean-Picture™III for spatial/temporal and Mosquito noise reduction
 - ◆ Pixel-Composer™III for following feature:
 - ◆ Inverse 3:2/2:2 pull-down for Film Mode detection
 - ◆ Motion Compensation de-interlace
 - ◆ Ultra-Zoom™

- ◆ Input color space conversion
- ◆ Vivid-Color™
- ◆ Digital hue, saturation, brightness and contrast adjustments
- ◆ Support DLTI/DCTI video-quality improvement
- ◆ Independent Color Manager
- ◆ Support Black/White Level Expansion and ACC
- ◆ Support 2D Y peaking filter and coring
- ◆ sRGB compliance and Gamma correction
- ◆ 3Dither™ serves as advanced dithering function
- OSD, sub-title Engine & Cursor
 - ◆ Powerful 3D GPU IMAGINATION **GE7800**
 - ◆ Support 4K2K OSD plane, sub-title Engine & Cursor respectively.
 - ◆ Additional 2D graphic engine
- **MEMC engine integration**
 - ◆ **Support 24Hz/25Hz/30Hz MEMC to 60Hz**
 - ◆ **Support film mode detection**
- Panel Interface
 - ◆ Built-in fully programmable display timing generator
 - ◆ Support up to 120Hz FHD with EPI , **CEDS**
 - ◆ Support up to 60Hz 4K2K with Vby1 8 lane Tx or 12 lanes EPI
 - ◆ Integrated high-quality Spread-Spectrum Display
 - ◆ Support up to 60Hz FPR/SG 3D panel
- System Controller
 - ◆ RISC processors for System control and audio/video control
 - ◆ Quad core ARM 64bits CPU with 1MB L2 Cache
- Memory Interface
 - ◆ Support eMMC 5.1 HS400
 - ◆ Configurable flash access timing
 - ◆ **Support internal DDR3 and external DDR3 (total up to 1.5GB)**
- Peripheral Interface
 - ◆ Low-speed Peripherals
 - ◆ Support two 16550 UARTs, each has 16-byte FIFO.
 - ◆ Support one IrDA Rx interface, which complies with NEC, SHARP, Sony SIRC protocol I, and Philips RC-5.
 - ◆ Support three parallel transport stream input/output and CI+ 1.4
 - ◆ Support 4x I2C master & two I2C Slave
 - ◆ Support up to 10 sets PWM output.
 - ◆ Support 3 Slow Speed ADC for bottom control
- High-speed Peripherals
 - ◆ USB 3.0 Host port x 1
 - ◆ USB 2.0 Host Ports x 2
 - ◆ Embedded 10/100 ETN MAC/PHY

- Basics
 - ◆ Single 27MHz crystal or OSC clock input with embedded PLLs.
 - ◆ 1.0V CPU power (PMU), 1.0V core power, 2.5V/3.3V analog power, 3.3V digital IO power and 1.5V DDR3
 - ◆ EDHS-PBGA 27x27

3 Pin list

3.1 Analog Power / Ground

Pin NO	Pin Name	Type	Description	Note
L8	STB3V3_1	AP	Standby LDO Input1 Power 3.3V	3.3V

AB9	STB3V3_2	AP	Standby LDO Input2 Power 3.3V	3.3V
U8,V8,W8,Y8	A3V3	AP	Analog IP 3.3V power supply	3.3V
AB8	HDRX3V3	AP	HDMI RX PHY 3.3V	3.3V
AB10	HDRX1V0	AP	HDMI RX PHY 1.0V	1.0V
H11	LV1V0	AP	Panel Interface 1.0V	1.0V
AB23	USB1V0	AP	USB2.0 / USB3.0 Power 1.0V	1.0V
H12,H13	LV1V5	AP	Panel Interface 1.5V	1.0V
H9	GHA1V0	AP	10/100 ETN PHY Power 1.0V	1.0V
H8	GHP1V0	AP	10/100 ETN PHY Power 1.0V	1.0V
R3	ADCG	AP	YPP ADC / Video DAC GND	GND
L5	BBG	AP	Base band Audio / IF ADC GND	GND

Note

1. AP : Analog Power/Ground

3.2 Digital Power / Ground

Pin NO	Pin Name	Type	Description	Note
A3,A18,A21,A23,A31,B18,B21,B23,C1,C17,C18,C21,C23,D3,D14,D17,D18,D21,D23,E4,E18,E21,E23,E24,E25,E26,E27,E28,F2,F3,F24,F25,F26,F28,G3,G28,H3,H7,H28,J7,J8,J28,K7,K28,K29,K30,L11,L12,L13,L14,L15,L16,L17,L18,L19,L20,L21,L22,L23,L28,M11,M12,M13,M14,M15,M16,M17,M18,M19,M20,M21,M22,M23,M28,N11,N12,N13,N14,N15,N16,N17,N18,N19,N20,N21,N22,N23,N28,P11,P12,P13,P14,P15,P16,P17,P18,P19,P20,P21,P22,P23,P28,R2,R11,R12,R13,R14,R15,R16,R17,R18,R19,R20,R21,R22,R23,R28,T3,T11,T12,T13,T14,T15,T16,T17,T18,T19,T20,T21,T22,T23,T28,T29,T30,T31,T32,U4,U11,U12,U13,U14,U15,U16,U17,U18,U19,U20,U21,U22,U23,V1,V3,V4,V5,V11,V12,V13,V14,V15,V16,V17,V18,V19,V20,V21,V22,V23,W5,W11,W12,W13,W14,W15,W16,W17,W18,W19,W20,W21,W22,W23,W30,Y1,Y5,Y11,Y12,Y13,Y14,Y15,Y16,Y17,Y18,Y19,Y20,Y21,Y22,Y23,Y30,AA2,AA30,AB1,AB3,AB26,AB30,AC23,AC24,AC27,AC30,AD24,AD27,AD30,AD32,AE5,AF5,AE19,AE20,AE21,AE24,AE25,AE30,AE32,AF19,AF20,AF24,AF25,AF26,AF28,AG1,AH2,AJ1,AJ2,AJ3,AJ4,AK2,AK3,AK4,AK5,AK6,AK7,AK8,AK9,AK10,AK11,AK12,AK13,AK14,AK15,AK16,AK17,AK18,AK19,AK20,AK21,AK22,AK23,AK24,AK25,AK26,AK27,AK28,AK29,AK30	DGND	DG	Digital GND	GND
A19,A20,B19,B20,C19,C20,D19,D20,E19,E20,J9,J10,J11,J12,J13,J14,J15,J16,J17,J18,J19,J20,J21,J22,K9,L9,M9,N9,P9,R9,T9,U9,V9,W9,Y9,AA9,AB19,AB20,AB21	CO1V0	DP	Core Power 1.0V	
T25,U25,V25,W25,U28,U29,U30,U31,U32,V28,V29,V30,V31,V32	CPU1V0	DP	SCPU Power 1.0V	
H10	GHD1V0	DP	Giga ETN Digital Power 1.0V	1.0V
N8,P8,R8,T8	D3V3	DP	General I/O Power 3.3V	3.3V
AA25	EMMC1V8	DP	EMMC I/O Power 1.8V	1.8V
A22,B22,C22,D22,E22,J24,J25,K25,L25,M25,N25,P25,R25,	DDR_1V5	DP	DDR I/O Power 1.5V	DDR3 1.5V only
Note 1. DP : Digital Power 2. DG: Digital Ground				

3.3 DDR3 Signal

Pin NO	Pin Name	Type	Description	Note
C26	DC1_A0	DDRO	DC1 ADDRESS BIT A0	
A29	DC1_A1	DDRO	DC1 ADDRESS BIT A1	
A26	DC1_A2	DDRO	DC1 ADDRESS BIT A2	
A25	DC1_A3	DDRO	DC1 ADDRESS BIT A3	
D29	DC1_A4	DDRO	DC1 ADDRESS BIT A4	
C25	DC1_A5	DDRO	DC1 ADDRESS BIT A5	
D28	DC1_A6	DDRO	DC1 ADDRESS BIT A6	
D25	DC1_A7	DDRO	DC1 ADDRESS BIT A7	
C28	DC1_A8	DDRO	DC1 ADDRESS BIT A8	
A27	DC1_A9	DDRO	DC1 ADDRESS BIT A9	
C30	DC1_A10	DDRO	DC1 ADDRESS BIT A10	
D27	DC1_A11	DDRO	DC1 ADDRESS BIT A11	
C29	DC1_A12	DDRO	DC1 ADDRESS BIT A12	
B27	DC1_A13	DDRO	DC1 ADDRESS BIT A13	
B29	DC1_A14	DDRO	DC1 ADDRESS BIT A14	
A30	DC1_A15	DDRO	DC1 ADDRESS BIT A15	
A24	DC1_BA0	DDRO	DC1 Bank ADDRESS BIT A0	
B30	DC1_BA1	DDRO	DC1 Bank ADDRESS BIT A1	
D26	DC1_BA2	DDRO	DC1 Bank ADDRESS BIT A2	
A28	DC1_CAS	DDRO	DC1 Column Address output (low Active)	
D30	DC1_CKE	DDRO	DC1 Clock Enable output	
K31	DC1_DM0	DDRO	DC1 Data Mask 1 output	
K32	DC1_DM1	DDRO	DC1 Data Mask 2 output	
D31	DC1_DM2	DDRO	DC1 Data Mask 3 output	
D32	DC1_DM3	DDRO	DC1 Data Mask 4 output	
P29	DC1_DQ0	DDRIO	DC1 DQ BIT 0	
L30	DC1_DQ1	DDRIO	DC1 DQ BIT 1	
R30	DC1_DQ2	DDRIO	DC1 DQ BIT 2	
L29	DC1_DQ3	DDRIO	DC1 DQ BIT 3	
P30	DC1_DQ4	DDRIO	DC1 DQ BIT 4	
M30	DC1_DQ5	DDRIO	DC1 DQ BIT 5	
R29	DC1_DQ6	DDRIO	DC1 DQ BIT 6	
M29	DC1_DQ7	DDRIO	DC1 DQ BIT 7	
L32	DC1_DQ8	DDRIO	DC1 DQ BIT 8	
P32	DC1_DQ9	DDRIO	DC1 DQ BIT 9	
L31	DC1_DQ10	DDRIO	DC1 DQ BIT 10	
P31	DC1_DQ11	DDRIO	DC1 DQ BIT 11	
M32	DC1_DQ12	DDRIO	DC1 DQ BIT 12	
R32	DC1_DQ13	DDRIO	DC1 DQ BIT 13	
M31	DC1_DQ14	DDRIO	DC1 DQ BIT 14	
R31	DC1_DQ15	DDRIO	DC1 DQ BIT 15	
H29	DC1_DQ16	DDRIO	DC1 DQ BIT 16	
E30	DC1_DQ17	DDRIO	DC1 DQ BIT 17	
J30	DC1_DQ18	DDRIO	DC1 DQ BIT 18	
E29	DC1_DQ19	DDRIO	DC1 DQ BIT 19	
H30	DC1_DQ20	DDRIO	DC1 DQ BIT 20	
F30	DC1_DQ21	DDRIO	DC1 DQ BIT 21	
J29	DC1_DQ22	DDRIO	DC1 DQ BIT 22	
F29	DC1_DQ23	DDRIO	DC1 DQ BIT 23	
E32	DC1_DQ24	DDRIO	DC1 DQ BIT 24	
H32	DC1_DQ25	DDRIO	DC1 DQ BIT 25	
E31	DC1_DQ26	DDRIO	DC1 DQ BIT 26	

H31	DC1_DQ27	DDRIO	DC1 DQ BIT 27	
F32	DC1_DQ28	DDRIO	DC1 DQ BIT 28	
J32	DC1_DQ29	DDRIO	DC1 DQ BIT 29	
F31	DC1_DQ30	DDRIO	DC1 DQ BIT 30	
J31	DC1_DQ31	DDRIO	DC1 DQ BIT 31	
N29	DC1_DQS0	DDRIO	DC1 Data Strobe 0 (+)	
N30	DC1_DQS0B	DDRIO	DC1 Data Strobe 0 (-)	
N32	DC1_DQS1	DDRIO	DC1 Data Strobe 1 (+)	
N31	DC1_DQS1B	DDRIO	DC1 Data Strobe 1 (-)	
G29	DC1_DQS2	DDRIO	DC1 Data Strobe 2 (+)	
G30	DC1_DQS2B	DDRIO	DC1 Data Strobe 2 (-)	
G32	DC1_DQS3	DDRIO	DC1 Data Strobe 3 (+)	
G31	DC1_DQS3B	DDRIO	DC1 Data Strobe 3 (-)	
B32	DC1_CLK	DDRO	DC1 CLK output (+)	
B31	DC1_CLKB	DDRO	DC1 CLK output (-)	
B25	DC1_ODT	DDRO	DC1 ODT output	
C27	DC1_RAS	DDRO	DC1 Row Address Output (Low Active)	
B26	DC1_RST	DDRO	DC1 Reset Output	
B28	DC1_WEN	DDRO	DC1 Write Enable Output (Low Active)	
C31	DC1_CSB_1	DDRO	DC1 Chip Select 1	
C32	DC1_CSB	DDRO	DC1 Chip Select 0	
B24	DC2_VREF	DDRI	DC2 VREF	
C24	ZQ	DDRI	DC1 ZQ Input	Connect 240R,1% to GND
D24	ZQ_1	DDRI	DC1 ZQ Input	Connect 240R,1% to GND
Note	1. DDRIO: DDR PHY I/O (Bi-direction) 2. DDRO: DDR PHY output 3. DDRI: DDR PHY input			

3.4 HDMI

Pin NO	Pin Name	Type	Description	Note
AL18	P0_CKN	AI	HDMI_RX_PORT 0_CLK_Pair1_Negative	Differential impedance 100 ohm
AM18	P0_CKP	AI	HDMI_RX_PORT 0_CLK_Pair1_Positive	
AL19	P0_BN	AI	HDMI_RX_PORT 0_Pair0_Negative	Differential impedance 100 ohm
AM19	P0_BP	AI	HDMI_RX_PORT 0_Pair0_Positive	Common Mode impedance 30ohm (*)
AL21	P0_GN	AI	HDMI_RX_PORT 0_Pair1_Negative	Differential impedance 100 ohm
AM21	P0_GP	AI	HDMI_RX_PORT 0_Pair1_Positive	
AM22	P0_RN	AI	HDMI_RX_PORT 0_Pair2_Negative	Differential impedance 100 ohm
AL22	P0_RP	AI	HDMI_RX_PORT 0_Pair2_Positive	
AL12	P1_CKN	AI	HDMI_RX_PORT 1_CLK_Pair1_Negative	Differential impedance 100 ohm
AM12	P1_CKP	AI	HDMI_RX_PORT 1_CLK_Pair1_Positive	
AL13	P1_BN	AI	HDMI_RX_PORT 1_Pair0_Negative	Differential impedance 100 ohm
AM13	P1_BP	AI	HDMI_RX_PORT 1_Pair0_Positive	Common Mode impedance 30ohm
AL15	P1_GN	AI	HDMI_RX_PORT 1_Pair1_Negative	Differential impedance 100 ohm
AM15	P1_GP	AI	HDMI_RX_PORT 1_Pair1_Positive	
AM16	P1_RN	AI	HDMI_RX_PORT 1_Pair2_Negative	Differential impedance 100 ohm
AL16	P1_RP	AI	HDMI_RX_PORT 1_Pair2_Positive	
AL6	P2_CKN	AI	HDMI_RX_PORT 2_CLK_Pair1_Negative	Differential impedance 100 ohm
AM6	P2_CKP	AI	HDMI_RX_PORT 2_CLK_Pair1_Positive	
AL7	P2_BN	AI	HDMI_RX_PORT 2_Pair0_Negative	Differential impedance 100 ohm
AM7	P2_BP	AI	HDMI_RX_PORT 2_Pair0_Positive	Common Mode impedance 30ohm
AL9	P2_GN	AI	HDMI_RX_PORT 2_Pair1_Negative	Differential impedance 100 ohm
AM9	P2_GP	AI	HDMI_RX_PORT 2_Pair1_Positive	
AM10	P2_RN	AI	HDMI_RX_PORT 2_Pair2_Negative	Differential impedance 100 ohm
AL10	P2_RP	AI	HDMI_RX_PORT 2_Pair2_Positive	
AK1	P3_CKN	AI	HDMI_RX_PORT 3_CLK_Pair1_Negative	Differential impedance 100 ohm
AL1	P3_CKP	AI	HDMI_RX_PORT 3_CLK_Pair1_Positive	
AL2	P3_BN	AI	HDMI_RX_PORT 3_Pair0_Negative	Differential impedance 100 ohm
AM2	P3_BP	AI	HDMI_RX_PORT 3_Pair0_Positive	Common Mode impedance 30ohm
AL3	P3_GN	AI	HDMI_RX_PORT 3_Pair1_Negative	Differential impedance 100 ohm
AM3	P3_GP	AI	HDMI_RX_PORT 3_Pair1_Positive	
AM4	P3_RN	AI	HDMI_RX_PORT 3_Pair2_Negative	Differential impedance 100 ohm
AL4	P3_RP	AI	HDMI_RX_PORT 3_Pair2_Positive	
AH1	REXT	AI	HDMI_REXT	
AG15	HDMI_CEC	AIO	CEC connection	
AL23	CBUS_RX	AI	MHL CBUS_RX circuit connection	
Note	AI: Analog Input AIO: Analog Input / Output			

3.5 EPI

Pin NO	Pin Name	Type	Description	Note
A4	EPI_TX12P	AIO	EPI lane12 positive data output Vby1 lane0 positive data output	
B4	EPI_TX12N	AIO	EPI lane12 negative data output Vby1 lane0 negative data output	
A5	EPI_TX13P	AIO	EPI lane13 positive data output Vby1 lane1 positive data output	
B5	EPI_TX13N	AIO	EPI lane13 negative data output Vby1 lane1 negative data output	
A6	EPI_TX14P	AIO	EPI lane14 positive data output Vby1 lane2 positive data output	
B6	EPI_TX14N	AIO	EPI lane14 negative data output Vby1 lane2 negative data output	
A7	EPI_TX15P	AIO	EPI lane15 positive data output Vby1 lane3 positive data output	
B7	EPI_TX15N	AIO	EPI lane15 negative data output Vby1 lane3 negative data output	
A8	EPI_TX16P	AIO	EPI lane16 positive data output Vby1 lane4 positive data output	
B8	EPI_TX16N	AIO	EPI lane16 negative data output Vby1 lane4 negative data output	
A9	EPI_TX17P	AIO	EPI lane17 positive data output Vby1 lane5 positive data output	
B9	EPI_TX17N	AIO	EPI lane17 negative data output Vby1 lane5 negative data output	
A10	EPI_TX18P	AIO	EPI lane18 positive data output Vby1 lane6 positive data output	
B10	EPI_TX18N	AIO	EPI lane18 negative data output Vby1 lane6 negative data output	
A11	EPI_TX19P	AIO	EPI lane19 positive data output Vby1 lane7 positive data output	
B11	EPI_TX19N	AIO	EPI lane19 negative data output Vby1 lane7 negative data output	
A12	EPI_TX20P	AIO	EPI lane20 positive data output Vby1 lane8 positive data output	
B12	EPI_TX20N	AIO	EPI lane20 negative data output Vby1 lane8 negative data output	
A13	EPI_TX21P	AIO	EPI lane21 positive data output Vby1 lane9 positive data output	
B13	EPI_TX21N	AIO	EPI lane21 negative data output Vby1 lane9 negative data output	
A14	EPI_TX22P	AIO	EPI lane22 positive data output Vby1 lane10 positive data output	
B14	EPI_TX22N	AIO	EPI lane22 negative data output Vby1 lane10 negative data output	
A15	EPI_TX23P	AIO	EPI lane23 positive data output Vby1 lane11 positive data output	
B15	EPI_TX23N	AIO	EPI lane23 negative data output Vby1 lane11 negative data output	
Note	AIO: Analog Input/Output AO: Analog Output			

3.6 USB 3.0

Pin NO	Pin Name	Type	Description	Note
AL28	HSIN2	AI	USB3.0_RX_Differential_Pair_Negative_2	Differential impedance 90 ohm
AM28	HSIP2	AI	USB3.0_RX_Differential_Pair_Positive_2	
AL27	HSOP	AO	USB3.0_TX_Differential_Pair_Negative	Differential impedance 90 ohm
AM27	HSON	AO	USB3.0_TX_Differential_Pair_Positive	
Note	AI: Analog Input AO: Analog Output			

3.7 USB 2.0

Pin NO	Pin Name	Type	Description	Note
G1	HSDM0	AIO	USB2.0_Differential_Pair_Negative	Differential impedance 90 ohm
G2	HSDP0	AIO	USB2.0_Differential_Pair_Positive	
AM24	HSDM1	AIO	USB2.0_Differential_Pair_Negative	Differential impedance 90 ohm
AL24	HSDP1	AIO	USB2.0_Differential_Pair_Positive	
AM25	HSDM2	AIO	USB2.0_Differential_Pair_Negative	Differential impedance 90 ohm
AL25	HSDP2	AIO	USB2.0_Differential_Pair_Positive	
AM30	HSDM3	AIO	USB2.0_Differential_Pair_Negative	Differential impedance 90 ohm
AL30	HSDP3	AIO	USB2.0_Differential_Pair_Positive	
Note	AIO: Analog Input / Output			

3.8 10/100M Ethernet

Pin NO	Pin Name	Type	Description	Note
E2	MDIN1	AIO	10/100M_ETN_Differential_Pair1_Negative	
E1	MDIP1	AIO	10/100M_ETN_Differential_Pair1_Positive	
D1	MDIN0	AIO	10/100M_ETN_Differential_Pair0_Negative	
D2	MDIP0	AIO	10/100M_ETN_Differential_Pair0_Positive	
Note	AIO: Analog Input / Output AI: Analog Input			

3.9 IF ADC

Pin NO	Pin Name	Type	Description	Note
W2	IP_1	AI	Zero IF I-channel ADC differential input positive	
W3	IN_1	AI	Zero IF I-channel ADC differential input negative	
Y2	QP_2	AI	Zero IF Q-channel ADC differential input positive	
Y3	QN_2	AI	Zero IF Q-channel ADC differential input negative	
U2	IFN_0	AI	IF ADC Differential Input Negative	
U3	IFP_0	AI	IF ADC Differential Input Positive	
Note	AI: Analog Input			

3.10 PLL/XTAL

Pin NO	Pin Name	Type	Description	Note
T2	XOUT	AO	27MHz XTAL clock output	
T1	XIN	AI	27MHz XTAL clock input	
AJ18	RTC_XO_USBOCD0	AO	RTC 32.768KHz clock output	
AJ19	RTC_XI_USBOCD1	AI	RTC 32.768KHz clock input	

Note	AO: Analog Output AI: Analog Input
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3.11 Video ADC /Sync/ SCART Input

Pin NO	Pin Name	Type	Description	Note
J3	VSYN	DIO	Vsync input	
J2	HSYN	DIO	Hsync input	
K2	VINBP	AI	YPbPr/VGA Blue Input Group1	
K3	VINBN_VIDCORE	AI	Common GND for YPbPr/VGA Group1	
L1	VINGP_Demod_reset	AI	YPbPr/VGA Green Input Group1	
L2	VINGN_DVS_I2C	AI	Common GND for YPbPr/VGA Group1	
M2	VINRP_Tuner0_rest	AI	YPbPr/VGA Red Input Group1	
M3	VINRN_VID_CPU/DVS_I2C	AI	Common GND for YPbPr/VGA Group1	
N3	VIN3P	AI	YPbPr/VGA Blue Input Group2	
P1	VINY0N	AI	Common GND for YPbPr/VGA Group2	
P2	VIN4P	AI	YPbPr/VGA Green Input Group2	
P3	VIN5P	AI	YPbPr/VGA Red Input Group2	
W5	VIN13P	AI	CVBS/S-Video C Input	
R5	VIN10P	AI	CVBS/S-Video Y Input	
R4	VINA0N	AI	Common Ground for CVBS/S-Video	
Note	AI : Analog Input AO : Analog Output AIO : Analog Input/Output DIO : Digital Input/Output			

3.12 Video Output

Pin NO	Pin Name	Type	Description	Note
H2	VDACOUT	AO	CVBS DAC output1	
J1	VDBSOUT_SC_PWR_SEL	AO	CVBS DAC output2 with analog bypass function	
Note	AO: Analog Output			

3.13 LSADC

Pin NO	Pin Name	Type	Description	Note
AH17	LS0	AIO	LSADC input 0 / GPIO	
AG17	LS1	AIO	LSADC input 1 / GPIO	
AJ16	LS2	AIO	LSADC input 2 / GPIO	
AG15	LS4	AIO	LSADC input 4 / GPIO	
AH16	LS6	AIO	LSADC input 6 / GPIO	
Note	AIO: Analog Input / Output AI: Analog Input			

3.14 Audio Input / Output

Pin list and application Notice

Pin NO	Pin Name	Type	Description	Note
N4	Gpio_36_HPOR	AO	Head Phone/Speaker output R	
N5	Gpio_36_HPOL	AO	Head Phone/Speaker output L	
P4	AIO2R_CMD_VCC_SC	AIO	Audio R DAC line output 2 and input	

P5	AIO2L_HP_DET	AIO	Audio L DAC line output 2 and input	
J4	AIO1R_AV2_DEMOD_DSC_22	AIO	Audio R DAC line output 1 and input	
H5	AIO1L_AV1_CVBS_DET	AIO	Audio L DAC line output 1 and input	
H4	AI3R_COMP1_DET	AI	Audio R ADC input 3	
G5	AI3L_AMP_SCL	AI	Audio L ADC input 3	
G4	AI2R_AMP_SDA	AI	Audio R ADC input 2	
P5	AI2L_AMP_RESET_N	AI	Audio L ADC input 2	
M4	AIN1R	AI	Audio R ADC input 1	
M5	AIN1L	AI	Audio L ADC input 1	
K5	Micbais	AO	MIC Bias Voltage output	
E3	GPIO_6_SPDIF_OUT_0	AO	Spdif output	
L4	VCMBB	AI	BaseBand Audio ADC Common mode voltage	Parallel 1uF/100nF to GND
Note	AI : Analog Input AO : Analog Output AIO : Analog Input/Output			

3.15 Reset

Pin NO	Pin Name	Type	Description	Note
AH15	RST	OD	Reset I/O (Open Drain)	Pull High with 10K
Note	OD: Open Drain			

3.16 Application for Analog Video Pin Assign

Following table is the pin assignment for LCD TV application. There are 4 ADC support all analog Video application such as VGA, Components, S-Video, and Composite video signal. It's recommended for designer to follow this table.

Pin NO	Pin Name	Description	Recommended Use
K2	VINBP	YPbPr/VGA Blue Input Group1	VGA Blue (+)
K3	VINBN_VIDCORE	Common GND for YPbPr/VGA Group1	VGA Common (-)
L1	VINGP_Demod_reset	YPbPr/VGA Green Input Group1	VGA Green (+)
L2	VINGN_DVS_I2C	Common GND for YPbPr/VGA Group1	VGA Common (-)
M2	VINRP_Tuner0_rest	YPbPr/VGA Red Input Group1	VGA Red (+)
M3	VINRN_VID_CPU/DVS_I2C	Common GND for YPbPr/VGA Group1	VGA Common (-)
N3	VIN3P	YPbPr/VGA Blue Input Group2	YPP1_Pb (+)
P1	VINY0N	Common GND for YPbPr/VGA Group2	YPP1_Common (-)
P2	VIN4P	YPbPr/VGA Green Input Group2	YPP1_Y (+)
P3	VIN5P	YPbPr/VGA Red Input Group2	YPP1_Pr (+)
P5	VIN13P	CVBS/S-Video C Input	CVBS (+) or SV_C(+)
R5	VIN_10P	CVBS/S-Video Y Input	CVBS (+) or SV_Y(+)
R4	VIN_A0N	Common Ground for CVBS/S-Video	CVBS Common (-) or SV Common (-)

3.17 TTL I/O and Pin Function Mux Table

Name	Pin no.	Driving Current	SMT	Power off Protection	5V Tolerance	Pin Share Function	ps_register
GPIO_0_DAC_SCLK	A17	4mA/8mA	1'b1	NO	NO	3: TCON_bit0,<O> 4: TCON_bit1,<O> 5: TCON_bit3,<O> 6: DISP_AVCOM_DAC_SCLK,<O>,<HS> 7: Id_spi0_p1_cs1,<O> 9: DEMOD_DSC_IN_src1,<I> F: MIS_GPIO_bit0,<I/O> def: MIS_GPIO_bit0,<I/O>	gpio_0_ps
GPIO_1_TCON_SDA/Tcon_5	B17	4mA/8mA	1'b1	YES	YES	3: TCON_bit10,<O> 4: TCON_bit11,<O> 5: TCON_bit12,<O> 7: Id_spi0_p2_sck_src1,<I/O> B: I2C1_SDA,<I/O> F: MIS_GPIO_bit1,<I/O> def: MIS_GPIO_bit1,<I/O>	gpio_1_ps
GPIO_2_TCON_SCL/TCON_9	A16	4mA/8mA	1'b1	YES	YES	3: TCON_bit20,<O> 4: TCON_bit21,<O> 5: TCON_bit22,<O> 7: Id_spi0_p3_sdo_SRC1,<I/O> B: I2C1_SCL,<I/O> F: MIS_GPIO_bit2,<I/O> def: MIS_GPIO_bit2,<I/O>	gpio_2_ps
GPIO_3_DAC_FS	C13	4mA/8mA	1'b1	NO	NO	3: TCON_bit4,<O> 4: TCON_bit5,<O> 5: TCON_bit6,<O> 6: DISP_AVCOM_DAC_FS,<O>,<HS> 8: I2S_out_Data0,<O> F: MIS_GPIO_bit3,<I/O> def: MIS_GPIO_bit3,<I/O>	gpio_3_ps
GPO_0_I2S_WCLK/SPDIF_OUT_1	D13	4mA/8mA	1'b1	YES	YES	3: TCON_bit0,<O> 4: TCON_bit1,<O> 5: TCON_bit2,<O> 7: I2S_out_WCLK,<O> 8: I2S_out_Data1,<O> 9: SPDIF_OUT_1,<O> F: MIS_GPO_bit0,<O> def: MIS_GPO_bit0,<O>	Gpo_0_ps
GPO_1_TCON_I2C_EN/Tcon_2	C12	4mA/8mA	1'b1	YES	YES	3: TCON_bit7,<O> 4: TCON_bit8,<O> 5: TCON_bit9,<O> 8: I2S_out_WCLK,<O> F: MIS_GPO_bit1,<O> def: MIS_GPO_bit1,<O>	Gpo_1_ps
GPIO_4_Vby_HTPD/Tcon_14	D12	4mA/8mA	1'b1	NO	NO	3: VBY1_HTPD_src1,<I> 4: TCON_bit14,<O> 5: TCON_bit25,<O> 6: EPI_LOCK_src1,<I>	gpio_4_ps

						7: Id_spi1_p1_cs1,<O> 8: I2S_out_MCLK,<O> F: MIS_GPIO_bit4,<I/O> def: MIS_GPIO_bit4,<I/O>	
GPIO_5_Vby_lock/Eplock	C11	4mA/8mA	1'b1	NO	NO	3: VBY1_LOCK_src1,<I> 4: TCON_bit15,<O> 5: TCON_bit35,<O> 6: EPI_LOCK_src0,<I> 7: Id_spi1_p2_sck_src1,<I/O> 8: I2S_out_SCLK,<O> 9: SPDIF_OUT,<O> F: MIS_GPIO_bit5,<I/O> def: MIS_GPIO_bit5,<I/O>	gpio_5_ps
GPIO_6_SPDIF_OUT_0	E3	4mA/8mA	1'b1	YES	YES	3: TCON_bit37,<O> 4: TCON_bit17,<O> 5: TCON_bit27,<O> 8: I2S_out_SCLK,<O> 9: SPDIF_OUT,<O> F: MIS_GPIO_bit6,<I/O> def: MIS_GPIO_bit6,<I/O>	gpio_6_ps
GPIO7_PMIC_RESET	D11	X	X	NO	NO	3: TCON_bit3,<O> 4: VBY1_HTPD_src2,<I> 5: TCON_bit5,<O> 7: Id_spi0_p4_sdi_SRC1,<I> B: I2C3_SDA_SRC2,<I/O> C: LVDS_A_GP,<AO> F: MIS_GPIO_bit7,<I/O> def: MIS_GPIO_bit7,<I/O>	lvds_a_gp_ps
GPIO08_Data_Format_0	C10	X	X	NO	NO	3: TCON_bit6,<O> 4: VBY1_LOCK_src2,<I> 5: TCON_bit8,<O> 7: Id_spi0_p5_v_sync,<O> B: I2C3_SCL_SRC2,<I/O> C: LVDS_A_GN,<AO> F: MIS_GPIO_bit8,<I/O> def: MIS_GPIO_bit8,<I/O>	lvds_a_gn_ps
GPIO09_DATA_FORMAT_1	D10	X	X	NO	NO	3: TCON_bit9,<O> 4: TCON_bit10,<O> 5: VBY1_HTPD_src0,<I> 7: Id_spi0_p6_h_sync,<O> C: LVDS_A_FP,<AO> F: MIS_GPIO_bit9,<I/O> def: MIS_GPIO_bit9,<I/O>	lvds_a_fp_ps
GPIO010_PWM_DIM_0	C9	X	X	NO	NO	3: Id_spi1_p6_h_sync,<O> 4: TCON_bit13,<O> 5: VBY1_LOCK_src0,<I> C: LVDS_A_FN,<AO> D: misc_pwm_0,<OD> F: MIS_GPIO_bit10,<I/O> def: MIS_GPIO_bit10,<I/O>	lvds_a_fn_ps
GPO011_PWM_DIM_1	D9	X	X	NO	NO	3: Id_spi1_p1_cs1,<O> 4: TCON_bit16,<O> 5: TCON_bit17,<O> B: I2C3_SCL_SRC1,<I/O> C: LVDS_A_EP,<AO> D: misc_pwm_1,<OD>	lvds_a_ep_ps

						F: MIS_GPIO_bit11,<I/O> def: MIS_GPIO_bit11,<I/O>	
GPO012_LD_SPI1_sck	C8	X	X	NO	NO	3: Id_spi1_p2_sck_src2,<I/O> 4: TCON_bit19,<O> 5: TCON_bit20,<O> B: I2C3_SDA_SRC1,<I/O> C: LVDS_A_EN,<AO> F: MIS_GPIO_bit12,<I/O> def: MIS_GPIO_bit12,<I/O>	lvds_a_en_p s
GPO013_LD_SPI1_sdo	D8	X	X	NO	NO	3: Id_spi1_p3_sdo_SRC1,<I/O> 4: TCON_bit22,<O> 5: TCON_bit23,<O> C: LVDS_A_DP,<AO> F: MIS_GPIO_bit13,<I/O> def: MIS_GPIO_bit13,<I/O>	lvds_a_dp_p s
GPO014_LD_SPI1_sync	C7	X	X	NO	NO	3: Id_spi1_p5_v_sync,<O> 4: TCON_bit25,<O> 5: Id_spi0_p6_h_sync,<O> 6: Id_spi1_p6_h_sync,<O> C: LVDS_A_DN,<AO> F: MIS_GPIO_bit14,<I/O> def: MIS_GPIO_bit14,<I/O>	lvds_a_dn_p s
GPIO_ACP	D7	X	X	NO	NO	3: TCON_bit17,<O> 4: TCON_bit18,<O> 5: TCON_bit19,<O> C: LVDS_A_CP,<AO> F: MIS_GPIO_bit141,<I/O> def: MIS_GPIO_bit141,<I/O>	lvds_a_cp_p s
GPIO_ACN	D6	X	X	NO	NO	3: TCON_bit3,<O> 4: TCON_bit4,<O> 5: TCON_bit5,<O> C: LVDS_A_CN,<AO> F: MIS_GPIO_bit142,<I/O> def: MIS_GPIO_bit142,<I/O>	lvds_a_cn_p s
GPIO_ABP	C6	X	X	NO	NO	3: TCON_bit18,<O> 4: TCON_bit19,<O> 5: TCON_bit20,<O> C: LVDS_A_BP,<AO> F: MIS_GPIO_bit143,<I/O> def: MIS_GPIO_bit143,<I/O>	lvds_a_bn_p s
GPIO_ABN	D5	X	X	NO	NO	3: TCON_bit9,<O> 4: TCON_bit10,<O> 5: TCON_bit11,<O> C: LVDS_A_BN,<AO> F: MIS_GPIO_bit144,<I/O> def: MIS_GPIO_bit144,<I/O>	lvds_a_bn_p s
GPIO_DEP	C5	X	X	NO	NO	3: TCON_bit12,<O> 4: TCON_bit13,<O> 5: TCON_bit14,<O> C: LVDS_D_EP,<AO> F: MIS_GPIO_bit145,<I/O> def: MIS_GPIO_bit145,<I/O>	lvds_d_ep_p s
GPIO_DEN	C4	X	X	NO	NO	3: TCON_bit23,<O> 4: TCON_bit24,<O> 5: TCON_bit25,<O> C: LVDS_D_EN,<AO> F: MIS_GPIO_bit146,<I/O>	lvds_d_en_p s

						def: MIS_GPIO_bit146,<I/O>	
GPIO15_D0	B3	X	X	NO	NO	3: Id_spi1_p4_sdi_SRC1,<I> 4: TCON_bit28,<O> 5: TCON_bit29,<O> C: LVDS_D_DP,<AO> D: I2S_out_Data0,<O> F: MIS_GPIO_bit15,<I/O> def: MIS_GPIO_bit15,<I/O>	lvds_d_dp_p s
GPIO16_D1	A2	X	X	NO	NO	3: Id_spi1_p5_v_sync,<O> 4: TCON_bit31,<O> 5: TCON_bit32,<O> C: LVDS_D_DN,<AO> D: I2S_out_Data1,<O> F: MIS_GPIO_bit16,<I/O> def: MIS_GPIO_bit16,<I/O>	lvds_d_dn_p s
GPIO017_D2	B2	X	X	NO	NO	3: TCON_bit33,<O> 4: TCON_bit34,<O> 5: TCON_bit35,<O> C: LVDS_D_CP,<AO> D: I2S_out_Data2,<O> F: MIS_GPIO_bit17,<I/O> def: MIS_GPIO_bit17,<I/O>	lvds_d_cp_p s
GPIO018_D3	D4	X	X	NO	NO	3: TCON_bit36,<O> 4: TCON_bit37,<O> 5: TCON_bit38,<O> C: LVDS_D_CN,<AO> D: I2S_out_Data3,<O> F: MIS_GPIO_bit18,<I/O> def: MIS_GPIO_bit18,<I/O>	lvds_d_cn_p s
GPIO019_DAC _Out	F4	X	X	NO	NO	3: TCON_bit39,<O> 4: TCON_bit0,<O> 5: TCON_bit1,<O> 6: DISP_AVCOM_DAC_Dout,<O>,< HS> 9: DEMOD_DSC_22_src1,<I/O> C: LVDS_D_BP,<AO> D: I2S_out_WCLK,<O> F: MIS_GPIO_bit19,<I/O> def: MIS_GPIO_bit19,<I/O>	lvds_d_bp_p s
GPIO020_MC LK	C3	X	X	NO	NO	3: TCON_bit16,<O> 4: TCON_bit17,<O> 5: TCON_bit18,<O> C: LVDS_D_BN,<AO> D: I2S_out_MCLK,<O> F: MIS_GPIO_bit20,<I/O> def: MIS_GPIO_bit20,<I/O>	lvds_d_bn_p s
GPIO021_SC LK	C2	X	X	NO	NO	3: TCON_bit5,<O> 4: TCON_bit15,<O> 5: TCON_bit25,<O> C: LVDS_D_AP,<AO> D: I2S_out_SCLK,<O> F: MIS_GPIO_bit21,<I/O> def: MIS_GPIO_bit21,<I/O>	lvds_d_ap_p s

GPIO022_SP DIF_OUT_1/ WCLK	B1	X	X	NO	NO	3: TCON_bit35,<O> 4: TCON_bit37,<O> 5: TCON_bit39,<O> 9: SPDIF_OUT_1,<O> C: LVDS_D_AN,<AO> D: I2S_out_WCLK,<O> F: MIS_GPIO_bit22,<I/O> def: MIS_GPIO_bit22,<I/O>	lvds_d_an_p s
AI2L_AMP_R ESET_N	F5	X	X	NO	NO	6: dmic_clk,<O> C: BB_AI2L,<AI> D: misc_pwm_0,<OD> F: MIS_GPIO_bit23,<I/O> def: BB_AI2L,<AI>	bb_ai2l_ps
AI2R_AMP_S DA	G4	X	X	NO	NO	6: dmic_clk_data_0,<I> B: I2C4_SDA_SRC0,<I/O> C: BB_AI2R,<AI> D: misc_pwm_1,<OD> F: MIS_GPIO_bit24,<I/O> def: BB_AI2R,<AI>	bb_ai2r_ps
AI3L_AMP_S CL	G5	X	X	NO	NO	B: I2C4_SCL_SRC0,<I/O> C: BB_AI3L,<AI> D: misc_pwm_2,<OD> F: MIS_GPIO_bit25,<I/O> def: BB_AI3L,<AI>	bb_ai3l_ps
AI3R_COMP1 _DET	H4	X	X	NO	NO	6: dmic_clk_data_1,<I> C: BB_AI3R,<AI> D: misc_pwm_3,<OD> F: MIS_GPIO_bit26,<I/O> def: BB_AI3R,<AI>	bb_ai3r_ps
AIO1L_AV1_ CVBS_DET	H5	X	X	NO	NO	C: BB_AIO1L,<AO> D: misc_pwm_4,<OD> F: MIS_GPIO_bit27,<I/O> def: BB_AIO1L,<AO>	bb_aio1l_ps
AIO1R_AV2_D EMOD_DSC_2 2	J4	X	X	NO	NO	3: TCON_bit4,<O> 4: TCON_bit9,<O> 5: TCON_bit13,<O> 9: DEMOD_DSC_POL,<OD> A: DEMOD_DSC_22_src2,<I/O> C: BB_AIO1R,<AO> D: misc_pwm_5,<OD> F: MIS_GPIO_bit28,<I/O> def: BB_AIO1R,<AO>	bb_aio1r_ps
AIO2L_HP_D ET	J5	X	X	NO	NO	9: ETN_LED_TXRX,<O> C: BB_AIO2L,<AO> F: MIS_GPIO_bit29,<I/O> def: BB_AIO2L,<AO>	bb_aio2l_ps
AIO2R_CMD_ VCC_SC	K4	X	X	NO	NO	9: ETN_LED_LINK,<O> C: BB_AIO2R,<AO> F: MIS_GPIO_bit30,<I/O> def: BB_AIO2R,<AO>	bb_aio2r_ps
Gpio_35_HP OL	N5	X	X	NO	NO	C: BB_HPOL,<AO> F: MIS_GPIO_bit31,<I/O> def: BB_HPOL,<AO>	bb_hpol_ps
Gpio_36_HP OR	N4	X	X	NO	NO	C: BB_HPOR,<AO> F: MIS_GPIO_bit32,<I/O> def: BB_HPOR,<AO>	bb_hpor_ps
VDBSOUT_S C_PWR_SEL	J1	X	X	NO	NO	7: Id_spi0_p6_h_sync,<O> C: vid_vdbs,<AO> F: MIS_GPIO_bit33,<I/O> def: vid_vdbs,<AO>	vdbs_out_ps

VDACOUT	H2	X	X	NO	NO	C: vid_vdac,<AO> F: MIS_GPIO_bit34,<I/O> def: vid_vdac,<AO>	vdac_out_ps
VSYNC	J3	X	X	NO	NO	0: nf_tmx_bit0,<I/O>,<HS> 3: TCON_bit20,<O> 4: TCON_bit1,<O> 5: TCON_bit2,<O> A: I2S_in_Data0,<I> C: VSYNC,<AI> D: misc_pwm_6,<OD> F: MIS_GPIO_bit35,<I/O> def: VSYNC,<AI>	vsync_ps
HSYNC	J2	X	X	NO	NO	0: nf_tmx_bit1,<I/O>,<HS> 3: TCON_bit18,<O> 4: TCON_bit19,<O> 5: TCON_bit20,<O> A: I2S_IN_WCLK,<I> C: HSYNC,<AI> D: misc_pwm_7,<OD> F: MIS_GPIO_bit36,<I/O> def: HSYNC,<AI>	hsync_ps
VINBP	K2	X	X	NO	NO	3: TCON_bit3,<O> 4: TCON_bit4,<O> 5: TCON_bit5,<O> A: I2S_in_MCLK,<I> C: VIN_0P,<AI> F: MIS_GPIO_bit37,<I/O> def: VIN_0P,<AI>	vin_0p_ps
VINBN_VIDCORE	K3	X	X	NO	NO	3: TCON_bit9,<O> 4: TCON_bit10,<O> 5: TCON_bit11,<O> A: I2S_IN_SCLK,<I> C: VIN_BN,<AI> F: MIS_GPIO_bit38,<I/O> def: VIN_BN,<AI>	vin_bn_ps
VINGP_Demo d_reset	L1	X	X	NO	NO	3: TCON_bit12,<O> 4: TCON_bit13,<O> 5: TCON_bit14,<O> A: I2S_in_Data1,<I> C: VIN_1P,<AI> F: MIS_GPIO_bit39,<I/O> def: VIN_1P,<AI>	vin_1p_ps
VINGN_DVS_I 2C	L2	X	X	NO	NO	0: nf_tmx_ce_n_bit0,<O>,<HS> 3: TCON_bit15,<O> 4: TCON_bit16,<O> 5: TCON_bit17,<O> A: I2S_in_Data2,<I> B: I2C5_SDA_SRC1,<I/O> C: VIN_GN,<AI> F: MIS_GPIO_bit40,<I/O>	vin_gp_ps

						def: VIN_GN,<AI>	
VINRP_Tuner0_rest	M2	X	X	NO	NO	3: TCON_bit6,<O> 4: TCON_bit7,<O> 5: TCON_bit8,<O> A: I2S_in_Data3,<I> C: VIN_2P,<AI> F: MIS_GPIO_bit41,<I/O> def: VIN_2P,<AI>	vin_2p_ps
VINRN_VID_C PU/DVS_I2C	M3	X	X	NO	NO	0: nf_tmx_ce_n_bit1,<O>,<HS> 3: TCON_bit18,<O> 4: TCON_bit19,<O> 5: TCON_bit20,<O> B: I2C5_SCL_SRC1,<I/O> C: VIN_RN,<AI> F: MIS_GPIO_bit42,<I/O> def: VIN_RN,<AI>	vin_rn_ps
VIN3P	N3	X	X	NO	NO	C: VIN_3P,<AI> F: MIS_GPIO_bit43,<I/O> def: VIN_3P,<AI>	vin_3p_ps
VINY0N	P1	X	X	NO	NO	C: VIN_y0n,<AI> F: MIS_GPIO_bit44,<I/O> def: VIN_y0n,<AI>	vin_y0n_ps
VIN4P	P2	X	X	NO	NO	C: VIN_4P,<AI> F: MIS_GPIO_bit45,<I/O> def: VIN_4P,<AI>	vin_4p_ps
VIN5P	P3	X	X	NO	NO	C: VIN_5p,<AI> F: MIS_GPIO_bit46,<I/O> def: VIN_5p,<AI>	vin_5p_ps
FWSW0_DE MOD_S_IF_A GC (LNB)	P4	X	X	NO	NO	8: Id_spi0_p5_v_sync,<O> 9: DEMOD_S_IF_AGC,<O> C: SCART_FSW_0,<AI> D: I2S_out_Data2,<O> F: MIS_GPIO_bit47,<I/O> def: SCART_FSW_0,<AI>	scart_fsw_0_ps
VIN13P	P5	X	X	NO	NO	C: VIN_13P,<AI> F: MIS_GPIO_bit48,<I/O> def: VIN_13P,<AI>	vin_13p_ps
VIN10P	R5	X	X	NO	NO	C: VIN_10P,<AI> F: MIS_GPIO_bit49,<I/O> def: VIN_10P,<AI>	vin_10p_ps
VINA0N	R4	X	X	NO	NO	C: VIN_a0n,<AI> F: MIS_GPIO_bit50,<I/O> def: VIN_a0n,<AI>	vin_a0n_ps
GPIO_51_Tu ner0_SDA	AA4	4mA/8mA	1'b1	YES	YES	B: I2C2_SDA_SRC0,<I/O> F: MIS_GPIO_bit51,<I/O> def: MIS_GPIO_bit51,<I/O>	gpio_51_ps
GPIO_52_Tu ner0_SCL	Y4	4mA/8mA	1'b1	YES	YES	B: I2C2_SCL_SRC0,<I/O> F: MIS_GPIO_bit52,<I/O> def: MIS_GPIO_bit52,<I/O>	gpio_52_ps
GPIO_53_Tu ner1_SDA	AC4	4mA/8mA	1'b1	YES	YES	3: TCON_bit14,<O> 4: TCON_bit24,<O> 5: TCON_bit34,<O> B: I2C3_SDA_SRC0,<I/O>	gpio_53_ps

						F: MIS_GPIO_bit53,<I/O> def: MIS_GPIO_bit53,<I/O>	
GPIO_54_Tuner1_SCL	AB4	4mA/8mA	1'b1	YES	YES	3: TCON_bit16,<O> 4: TCON_bit6,<O> 5: TCON_bit1,<O> B: I2C3_SCL_SRC0,<I/O> F: MIS_GPIO_bit54,<I/O> def: MIS_GPIO_bit54,<I/O>	gpio_54_ps
GPIO_55_RF_IF_AGC1	W4	4mA/8mA	1'b1	YES	YES	3: ATV_IF_AGC,<OD> 4: DEMOD_IF_AGC,<O> 6: ATV_RF_AGC,<OD> 8: ETN_LED_LINK,<O> 9: ETN_LED_TXRX,<O> F: MIS_GPIO_bit55,<I/O> def: MIS_GPIO_bit55,<I/O>	gpio_55_ps
GPIO_56_TP0_SYC	AA3	4mA/8mA	1'b1	YES	YES	0: nf_tmx_bit2,<I/O>,<HS> 1: TP0_SYNC,<I>,<HS> 3: TCON_bit5,<O> 4: TCON_bit15,<O> 5: TCON_bit25,<O> F: MIS_GPIO_bit56,<I/O> def: MIS_GPIO_bit56,<I/O>	gpio_56_ps
GPIO_57_TP0_CLK	AB2	4mA/8mA	1'b1	YES	YES	0: nf_tmx_bit3,<I/O>,<HS> 1: TP0_CLK,<I>,<HS>,<AND> 3: TCON_bit9,<O> 4: TCON_bit19,<O> 5: TCON_bit29,<O> F: MIS_GPIO_bit57,<I/O> def: MIS_GPIO_bit57,<I/O>	gpio_57_ps
GPIO_58_TP0_VAL	AC2	4mA/8mA	1'b1	YES	YES	0: nf_tmx_bit4,<I/O>,<HS> 1: TP0_VAL,<I>,<HS> 3: TCON_bit11,<O> 4: TCON_bit21,<O> 5: TCON_bit31,<O> F: MIS_GPIO_bit58,<I/O> def: MIS_GPIO_bit58,<I/O>	gpio_58_ps
GPIO_59_TP0_D0	AC3	4mA/8mA	1'b1	YES	YES	0: nf_tmx_bit5,<I/O>,<HS> 1: TP0_Data_bit0,<I>,<HS> 3: TCON_bit1,<O> 4: TCON_bit11,<O> 5: TCON_bit21,<O> F: MIS_GPIO_bit59,<I/O> def: MIS_GPIO_bit59,<I/O>	gpio_59_ps
GPIO_60_TP0_D1	AD1	4mA/8mA	1'b1	YES	YES	0: nf_tmx_bit6,<I/O>,<HS> 1: TP0_Data_bit1,<I>,<HS> 2: SD_CD_src0,<I>,<HS> 3: TCON_bit6,<O> 4: TCON_bit16,<O> 5: TCON_bit26,<O> F: MIS_GPIO_bit60,<I/O> def: MIS_GPIO_bit60,<I/O>	gpio_60_ps
GPIO_61_TP0_D2	AD2	4mA/8mA	1'b1	YES	YES	0: nf_tmx_bit7,<I/O>,<HS> 1: TP0_Data_bit2,<I>,<HS> 2: SD_WP_src0,<I>,<HS> 3: TCON_bit12,<O> 4: TCON_bit22,<O> 5: TCON_bit32,<O> F: MIS_GPIO_bit61,<I/O> def: MIS_GPIO_bit61,<I/O>	gpio_61_ps

GPIO_62_TP0_D3	AD3	4mA/8mA	1'b1	YES	YES	0: nf_tmx_cle,<O>,<HS> 1: TP0_Data_bit3,<I>,<HS> 2: SD_CLK,<O>,<HS> 3: TCON_bit13,<O> 4: TCON_bit23,<O> 5: TCON_bit33,<O> F: MIS_GPIO_bit62,<I/O> def: MIS_GPIO_bit62,<I/O>	gpio_62_ps
GPIO_63_TP0_D4	AE2	4mA/8mA	1'b1	YES	YES	0: tmx_nf_rdy,<I>,<HS> 1: TP0_Data_bit4,<I>,<HS> 2: SD_CMD_src0,<I/O>,<HS> 3: TCON_bit16,<O> 4: TCON_bit26,<O> 5: TCON_bit36,<O> 7: I2S_out_Data3,<O> E: test_en_bit0,<I/O> F: MIS_GPIO_bit63,<I/O> def: MIS_GPIO_bit63,<I/O>	gpio_63_ps
GPIO_64_TP0_D5	AE3	4mA/8mA	1'b1	YES	YES	0: nf_tmx_rd_n,<O>,<HS> 1: TP0_Data_bit5,<I>,<HS> 2: SD_Data2_src0,<I/O>,<HS> 3: TCON_bit17,<O> 4: TCON_bit27,<O> 5: TCON_bit37,<O> 7: I2S_out_SCLK,<O> E: test_en_bit1,<I/O> F: MIS_GPIO_bit64,<I/O> def: MIS_GPIO_bit64,<I/O>	gpio_64_ps
GPIO_65_TP0_D6	AF1	4mA/8mA	1'b1	YES	YES	0: nf_tmx_wr_n,<O>,<HS> 1: TP0_Data_bit6,<I>,<HS> 2: SD_Data1_src0,<I/O>,<HS> 3: TCON_bit18,<O> 4: TCON_bit28,<O> 5: TCON_bit38,<O> 7: I2S_out_MCLK,<O> E: test_en_bit2,<I/O> F: MIS_GPIO_bit65,<I/O> def: MIS_GPIO_bit65,<I/O>	gpio_65_ps
GPIO_66_TP0_D7	AF2	4mA/8mA	1'b1	YES	YES	0: nf_tmx_ale,<O>,<HS> 1: TP0_Data_bit7,<I>,<HS> 2: SD_Data3_src0,<I/O>,<HS> 3: TCON_bit3,<O> 4: TCON_bit13,<O> 5: TCON_bit23,<O> 7: I2S_out_WCLK,<O> E: test_en_bit3,<I/O> F: MIS_GPIO_bit66,<I/O> def: MIS_GPIO_bit66,<I/O>	gpio_66_ps
TEST_07	AB5	4mA/8mA	1'b1	YES	YES	1: TP2_Data_bit0,<I>,<HS> 3: TCON_bit15,<O> 4: TCON_bit5,<O> 5: TCON_bit25,<O> 7: Id_spi0_p4_sdi_SRC0,<I> A: I2S_out_Data3,<O> C: misc_pwm_6,<OD> D: misc_pwm_3,<OD> E: test_en_bit4,<I/O> F: MIS_GPIO_bit70,<I/O> def: MIS_GPIO_bit70,<I/O>	gpio_70_ps

GPIO_71_TP2_D1/Tcon	AF3	4mA/8mA	1'b1	YES	YES	1: TP2_Data_bit1,<I>,<HS> 2: DISP_AVCOM_DAC_SCLK,<O>,<HS> 3: TCON_bit26,<O> 4: TCON_bit27,<O> 5: ATV_IF_AGC,<OD> 6: DEMOD_IF_AGC,<O> 7: Id_spi0_p5_v_sync,<O> 8: ATV_RF_AGC,<OD> A: I2S_out_WCLK,<O> C: misc_pwm_7,<OD> D: misc_pwm_4,<OD> F: MIS_GPIO_bit71,<I/O> def: MIS_GPIO_bit71,<I/O>	gpio_71_ps
TEST_08	AC5	4mA/8mA	1'b1	YES	YES	1: TP2_Data_bit2,<I>,<HS> 2: DISP_AVCOM_DAC_FS,<O>,<HS> 3: TCON_bit23,<O> 4: TCON_bit3,<O> 5: ATV_IF_AGC,<OD> 6: DEMOD_IF_AGC,<O> 7: Id_spi0_p6_h_sync,<O> 8: ATV_RF_AGC,<OD> A: I2S_out_MCLK,<O> C: misc_pwm_0,<OD> D: misc_pwm_5,<OD> E: test_en_bit5,<I/O> F: MIS_GPIO_bit72,<I/O> def: MIS_GPIO_bit72,<I/O>	gpio_72_ps
GPIO_73_TP2_D3/Tcon	AG2	4mA/8mA	1'b1	YES	YES	1: TP2_Data_bit3,<I>,<HS> 3: TCON_bit28,<O> 4: TCON_bit29,<O> 5: TCON_bit33,<O> 6: DEMOD_S_IF_AGC,<O> 7: Id_spi1_p1_cs1,<O> 8: uart2_tx,<OD> 9: ETN_LED_TXRX,<O> A: I2S_out_SCLK,<O> C: misc_pwm_1,<OD> D: misc_pwm_6,<OD> E: test_en_bit6,<I/O> F: MIS_GPIO_bit73,<I/O> def: MIS_GPIO_bit73,<I/O>	gpio_73_ps
TEST_09	AD5	4mA/8mA	1'b1	YES	YES	1: TP2_Data_bit4,<I>,<HS> 2: DISP_AVCOM_DAC_Dout,<O>,<HS> 4: TCON_bit15,<O> 5: TCON_bit13,<O> 6: DEMOD_S_IF_AGC,<O> 7: Id_spi1_p2_sck_src0,<I/O> 8: uart2_rxd_src0,<I> 9: ETN_LED_LINK,<O> C: misc_pwm_2,<OD> D: misc_pwm_7,<OD> E: test_en_bit7,<I/O> F: MIS_GPIO_bit74,<I/O> def: MIS_GPIO_bit74,<I/O>	gpio_74_ps

GPIO_75_TP2_D5/Tcon	AG3	4mA/8mA	1'b1	YES	YES	1: TP2_Data_bit5,<I>,<HS> 3: TCON_bit34,<O> 4: TCON_bit35,<O> 5: TCON_bit36,<O> 6: DEMOD_DSC_POL,<OD> 7: Id_spi1_p3_sdo_SRC0,<I/O> 8: uart2_cts_n,<I> C: misc_pwm_5,<OD> D: misc_pwm_0,<OD> E: test_en_bit8,<I/O> F: MIS_GPIO_bit75,<I/O> def: MIS_GPIO_bit75,<I/O>	gpio_75_ps
GPIO_76_TP2_D6/Tcon	AH3	4mA/8mA	1'b1	YES	YES	1: TP2_Data_bit6,<I>,<HS> 3: TCON_bit37,<O> 4: TCON_bit38,<O> 5: TCON_bit39,<O> 6: DEMOD_DSC_IN_src0,<I> 7: Id_spi1_p4_sdi_src0,<I> 8: uart2_rts_n,<O> C: misc_pwm_6,<OD> D: misc_pwm_1,<OD> E: test_en_bit9,<I/O> F: MIS_GPIO_bit76,<I/O> def: MIS_GPIO_bit76,<I/O>	gpio_76_ps
GPIO_77_TP2_D7/Tcon	AE4	4mA/8mA	1'b1	YES	YES	1: TP2_Data_bit7,<I>,<HS> 3: TCON_bit13,<O> 4: TCON_bit26,<O> 5: TCON_bit39,<O> 6: DEMOD_DSC_22_src0,<I/O> 7: Id_spi1_p5_v_sync,<O> C: misc_pwm_7,<OD> D: misc_pwm_2,<OD> E: test_en_bit10,<I/O> F: MIS_GPIO_bit77,<I/O> def: MIS_GPIO_bit77,<I/O>	gpio_77_ps
ST_GPIO_00_WOL_WAKE_UP	AH4	4mA/8mA	1'b1	YES	YES	2: ST_dbg_bit2,<I/O> 3: SD_Data0_src0,<I/O>,<HS> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit00,<I/O> def: ISO_MIS_GPIO_bit00,<I/O>	st_gpio_00_ps
ST_GPIO_01_VGA_SCL	AG5	4mA/8mA	1'b1	YES	YES	5: VDDC_SCL,<I> 6: uart1_tx,<OD> 7: Dispd_rgbw_dbg_uart_tx,<O> 8: emcu_ur_tx,<O> A: UARTRbus_TX,<O> C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPIO_bit01,<I/O> def: ISO_MIS_GPIO_bit01,<I/O>	st_gpio_01_ps
ST_GPIO_02_VGA_SDA	AH5	4mA/8mA	1'b1	YES	YES	5: VDDC_SDA,<I/O> 6: uart1_rxd_src0,<I> 7: Dispd_rgbw_dbg_gpio_src0,<I/O> 8: emcu_ur_rx_src1,<I> A: UARTRbus_RX_src1,<I> C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPIO_bit02,<I/O> def: ISO_MIS_GPIO_bit02,<I/O>	st_gpio_02_ps
TEST_05	AG4	4mA/8mA	1'b1	YES	YES	3: TCON_bit12,<O> 4: TCON_bit16,<O>	st_gpio_03_ps

						5: TCON_bit20,<O> B: I2C5_SDA_src0,<I/O> C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPIO_bit03,<I/O> def: ISO_MIS_GPIO_bit03,<I/O>	
TEST_06	AF4	4mA/8mA	1'b1	YES	YES	3: TCON_bit9,<O> 4: TCON_bit13,<O> 5: TCON_bit17,<O> B: I2C5_SCL_src0,<I/O> C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPIO_bit04,<I/O> def: ISO_MIS_GPIO_bit04,<I/O>	st_gpio_04_ps
ST_GPIO_05_I R_RX	AG6	4mA/8mA	1'b1	NO	NO	3: TCON_bit3,<O> 4: TCON_bit7,<O> 5: TCON_bit11,<O> 7: Dispdrgbw_dbg_gpio_src1,<I/O> > 8: IRRX,<I> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit05,<I/O> def: ISO_MIS_GPIO_bit05,<I/O>	st_gpio_05_ps
ST_GPIO_06 _H3 HPD	AH6	4mA/8mA	1'b1	YES	YES	C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit06,<I/O> def: ISO_MIS_GPIO_bit06,<I/O>	st_gpio_06_ps
ST_GPIO_07 _5V_DET_HDMI_3	AJ6	4mA/8mA	1'b1	YES	YES	C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPIO_bit07,<I/O> def: ISO_MIS_GPIO_bit07,<I/O>	st_gpio_07_ps
ST_GPIO_08 _H3_SDA	AG7	4mA/8mA	1'b1	YES	YES	5: HDDC3_SDA,<I/O> 8: uart2_tx,<OD> A: UARTRbus_TX,<O> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit08,<I/O> def: ISO_MIS_GPIO_bit08,<I/O>	st_gpio_08_ps
ST_GPIO_09 _H3_SCL	AH7	4mA/8mA	1'b1	YES	YES	5: HDDC3_SCL,<I> 8: uart2_rxd_src1,<I> A: UARTRbus_RX_src5,<I> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit09,<I/O> def: ISO_MIS_GPIO_bit09,<I/O>	st_gpio_09_ps
ST_GPIO_10 _5V_DET_HDMI_2	AG8	4mA/8mA	1'b1	YES	YES	2: ST_dbg_bit15,<I/O> 3: EJTAG_TDO,<O> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit10,<I/O> def: ISO_MIS_GPIO_bit10,<I/O>	st_gpio_10_ps
ST_GPIO_11 _H2_HPDI	AH8	4mA/8mA	1'b1	YES	YES	2: ST_dbg_bit3,<I/O> C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPIO_bit11,<I/O> def: ISO_MIS_GPIO_bit11,<I/O>	st_gpio_11_ps
ST_GPIO_12 _H2_SDA	AJ8	4mA/8mA	1'b1	YES	YES	2: ST_dbg_bit14,<I/O> 3: EJTAG_TDI_src1,<I> 5: HDDC2_SDA,<I/O> 8: uart2_tx,<OD> A: UARTRbus_TX,<O> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit12,<I/O> def: ISO_MIS_GPIO_bit12,<I/O>	st_gpio_12_ps

ST_GPIO_13_H2_SCL	AG9	4mA/8mA	1'b1	YES	YES	2: ST_dbg_bit13,<I/O> 3: EJTAG_TRST_src1,<I> 5: HDDC2_SCL,<I> 8: uart2_rxd_src2,<I> A: UARTRbus_RX_src2,<I> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit13,<I/O> def: ISO_MIS_GPIO_bit13,<I/O>	st_gpio_13_ps
ST_GPIO_14_H1_HPDP	AH9	4mA/8mA	1'b1	YES	YES	2: ST_dbg_bit11,<I/O> C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPIO_bit14,<I/O> def: ISO_MIS_GPIO_bit14,<I/O>	st_gpio_14_ps
ST_GPIO_15_5V_DET_HDMI_1	AG10	4mA/8mA	1'b1	YES	YES	2: ST_dbg_bit4,<I/O> C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPIO_bit15,<I/O> def: ISO_MIS_GPIO_bit15,<I/O>	st_gpio_15_ps
ST_GPIO_16_H1_SDA	AH10	X	1'b1	YES	YES	2: ST_dbg_bit10,<I/O> 3: EJTAG_TCLK_CLK_src1,<I>,<AND> 5: HDDC1_SDA,<I/O> 8: uart2_tx,<OD> A: UARTRbus_TX,<O> C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPIO_bit16,<I/O> def: ISO_MIS_GPIO_bit16,<I/O>	st_gpio_16_ps
ST_GPIO_17_H1_SCL	AJ10	X	1'b1	YES	YES	2: ST_dbg_bit12,<I/O> 3: EJTAG_TMS_src1,<I> 5: HDDC1_SCL,<I> 8: uart2_rxd_src3,<I> A: UARTRbus_RX_src3,<I> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit17,<I/O> def: ISO_MIS_GPIO_bit17,<I/O>	st_gpio_17_ps
ST_GPIO_18_H0_HPDP	AG11	X	1'b1	YES	YES	2: ST_dbg_bit7,<I/O> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit18,<I/O> def: ISO_MIS_GPIO_bit18,<I/O>	st_gpio_18_ps
ST_GPIO_19_5V_DET_HDMI_0	AH11	X	1'b1	YES	YES	2: ST_dbg_bit5,<I/O> C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPIO_bit19,<I/O> def: ISO_MIS_GPIO_bit19,<I/O>	st_gpio_19_ps
ST_GPIO_20_H0_SDA	AG12	4mA/8mA	1'b1	YES	YES	2: ST_dbg_bit9,<I/O> 5: HDDC0_SDA,<I/O> 8: uart2_tx,<OD> A: UARTRbus_TX,<O> C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPIO_bit20,<I/O> def: ISO_MIS_GPIO_bit20,<I/O>	st_gpio_20_ps
ST_GPIO_21_H0_SCL	AH12	4mA/8mA	1'b1	YES	YES	2: ST_dbg_bit8,<I/O> 5: HDDC0_SCL,<I> 8: uart2_rxd_src4,<I> A: UARTRbus_RX_src4,<I> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit21,<I/O> def: ISO_MIS_GPIO_bit21,<I/O>	st_gpio_21_ps

ST_GPIO_22_5V_HDMI_MHL	AJ1 2	4mA/8mA	1'b1	YES	YES	2: ST_dbg_bit6,<I/O> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit22,<I/O> def: ISO_MIS_GPIO_bit22,<I/O>	st_gpio_22_ps
ST_GPIO_23_H0_ARC	AG1 3	4mA/8mA	1'b1	YES	YES	9: SPDIF_OUT_1,<O> C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPIO_bit23,<I/O> def: ISO_MIS_GPIO_bit23,<I/O>	st_gpio_23_ps
ST_GPO_0_Tcon	AG1 8	4mA/8mA	1'b1	YES	YES	3: TCON_bit37,<O> 4: TCON_bit17,<O> 5: TCON_bit2,<O> 7: Dispdrgbw_dbg_uart_tx,<O> A: IRTX,<O> C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPO_bit0,<O> def: ISO_MIS_GPO_bit0,<O>	st_gpo_00_ps
ST_GPIO_24_uart0/1	AH1 3	4mA/8mA	1'b1	YES	YES	6: uart0_tx,<OD> 7: uart1_tx,<OD> 8: emcu_ur_tx,<O> A: UARTRbus_TX,<O> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit24,<I/O> def: ISO_MIS_GPIO_bit24,<I/O>	st_gpio_24_ps
ST_GPIO_25_uart0/1	AG1 4	4mA/8mA	1'b1	YES	YES	6: uart0_rxd,<I> 7: uart1_rxd_src1,<I> 8: emcu_ur_rx_src0,<I> A: UARTRbus_RX_src0,<I> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit25,<I/O> def: ISO_MIS_GPIO_bit25,<I/O>	st_gpio_25_ps
ST_GPIO_26_Micro_SDA	AH1 4	4mA/8mA	1'b1	YES	YES	2: ST_dbg_bit1,<I/O> B: I2C0_SDA,<I/O> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit26,<I/O> def: ISO_MIS_GPIO_bit26,<I/O>	st_gpio_26_ps
ST_GPIO_27_Micro_SCL	AJ1 4	4mA/8mA	1'b1	YES	YES	2: ST_dbg_bit0,<I/O> B: I2C0_SCL,<I/O> C: iso_misc_pwm_1,<OD> F: ISO_MIS_GPIO_bit27,<I/O> def: ISO_MIS_GPIO_bit27,<I/O>	st_gpio_27_ps
ST_GPIO_28_USBOCD2	AH1 8	4mA/8mA	1'b1	NO	NO	7: USB_PWR_FLAG1,<I> 9: SPDIF_IN,<I> C: iso_misc_pwm_0,<OD> F: ISO_MIS_GPIO_bit28,<I/O> def: ISO_MIS_GPIO_bit28,<I/O>	st_gpio_28_ps
LS6	AG1 6	X	X	NO	NO	C: lsadc6,<AI> F: ISO_MIS_GPIO_bit34,<I/O> def: lsadc6,<AI>	Lsadc6_ps
LS4	AG1 6	X	X	NO	NO	C: lsadc4,<AI> F: ISO_MIS_GPIO_bit33,<I/O> def: lsadc4,<AI>	Lsadc4_ps
LS2	AJ1 6	X	X	NO	NO	C: lsadc2,<AI> F: ISO_MIS_GPIO_bit32,<I/O> def: lsadc2,<AI>	Lsadc2_ps
LS1	AG1	X	X	NO	NO	C: lsadc1,<AI>	Lsadc1_ps

	7					F: ISO_MIS_GPIO_bit31,<I/O> def: lsadc1,<AI>	
LS0	AH1 7	X	X	NO	NO	C: lsadc0,<AI> F: ISO_MIS_GPIO_bit30,<I/O> def: lsadc0,<AI>	Lsadc0_ps
RTC_Xi_USB OCD1	AG1 9	X	X	NO	NO	8: USB_PWR_FLAG0,<I> C: RTC_XTLI,<AI> F: ISO_MIS_GPI_bit1,<I> def: RTC_XTLI,<AI>	rtc_xtl1_ps
RTC_XO_US BOCD0	AJ1 8	X	X	NO	NO	7: USB3_PWR_FLAG0,<I> C: RTC_XTLO,<AO> F: ISO_MIS_GPI_bit0,<I> def: RTC_XTLO,<AO>	grtc_xtlo_ps
GPIO_78_US B_pwr1_sd_c d	AH1 9	4mA/8mA	1'b1	YES	YES	8: USB_PWR_CTRL0,<O> C: misc_pwm_1,<OD> D: misc_pwm_7,<OD> F: MIS_GPIO_bit78,<I/O> def: MIS_GPIO_bit78,<I/O>	gpio_78_ps
GPIO_79_US B_pwr0_sd_w p	AG2 0	4mA/8mA	1'b1	YES	YES	6: USB3_PWR_CTRL0,<O> B: I2C4_SDA_src1,<I/O> C: misc_pwm_0,<OD> D: misc_pwm_6,<OD> F: MIS_GPIO_bit79,<I/O> def: MIS_GPIO_bit79,<I/O>	gpio_79_ps
GPIO_80_US B_pwr2_sd_d 1	AH2 0	4mA/8mA	1'b1	YES	YES	8: USB_PWR_CTRL1,<O> B: I2C4_SCL_src1,<I/O> C: misc_pwm_2,<OD> D: misc_pwm_3,<OD> F: MIS_GPIO_bit80,<I/O> def: MIS_GPIO_bit80,<I/O>	gpio_80_ps
GPIO_81_PC _IREQ_N_5V	AJ2 0	4mA/8mA	1'b1	YES	YES	1: PCMCIA_IREQ0_N,<I>,<HS> F: MIS_GPIO_bit81,<I/O> def: MIS_GPIO_bit81,<I/O>	gpio_81_ps
GPIO_82_PC _CD1_N	AG2 1	4mA/8mA	1'b1	YES	YES	1: PCMCIA_CD0_N,<I>,<HS> F: MIS_GPIO_bit82,<I/O> def: MIS_GPIO_bit82,<I/O>	gpio_82_ps
GPIO_83_PC _D3	AH2 1	4mA/8mA	1'b1	YES	YES	1: PCMCIA_D_bit3,<I/O>,<HS> F: MIS_GPIO_bit83,<I/O> def: MIS_GPIO_bit83,<I/O>	gpio_83_ps

GPIO_84_TP 1_D3	AG2 2	4mA/8mA	1'b1	YES	YES	1: TP1_Data_bit3,<I>,<HS> F: MIS_GPIO_bit84,<I/O> def: MIS_GPIO_bit84,<I/O>	gpio_84_ps
GPIO_85_PC _D4	AH2 2	4mA/8mA	1'b1	YES	YES	1: PCMCIA_D_bit4,<I/O>,<HS> 9: TPO_data_bit0_pad,<O>,<HS> A: HIF_Data_bit1,<I/O> F: MIS_GPIO_bit85,<I/O> def: MIS_GPIO_bit85,<I/O>	gpio_85_ps
GPIO_86_TP 1_D4	AJ2 2	4mA/8mA	1'b1	YES	YES	1: TP1_Data_bit4,<I>,<HS> 8: SC_DATA,<I/O> A: HIF_Data_bit2,<I/O> F: MIS_GPIO_bit86,<I/O> def: MIS_GPIO_bit86,<I/O>	gpio_86_ps
GPIO_87_PC _D5	AG2 3	4mA/8mA	1'b1	YES	YES	1: PCMCIA_D_bit5,<I/O>,<HS> 8: SC_RST,<OD> 9: TPO_data_bit1_pad,<O>,<HS> A: HIF_Data_bit3,<I/O> F: MIS_GPIO_bit87,<I/O> def: MIS_GPIO_bit87,<I/O>	gpio_87_ps
GPIO_88_TP 1_D5	AH2 3	4mA/8mA	1'b1	YES	YES	1: TP1_Data_bit5,<I>,<HS> 8: SC_SCLK,<OD> A: HIF_Data_bit4,<I/O> F: MIS_GPIO_bit88,<I/O> def: MIS_GPIO_bit88,<I/O>	gpio_88_ps
GPIO_89_PC _D6	AG2 4	4mA/8mA	1'b1	YES	YES	1: PCMCIA_D_bit6,<I/O>,<HS> 8: SC_CD,<I> 9: TPO_data_bit2_pad,<O>,<HS> A: HIF_Data_bit5,<I/O> F: MIS_GPIO_bit89,<I/O> def: MIS_GPIO_bit89,<I/O>	gpio_89_ps
GPIO_90_TP 1_D6	AH2 4	4mA/8mA	1'b1	YES	YES	1: TP1_Data_bit6,<I>,<HS> A: HIF_Data_bit6,<I/O> F: MIS_GPIO_bit90,<I/O> def: MIS_GPIO_bit90,<I/O>	gpio_90_ps
GPIO_91_PC _D7	AJ2 4	4mA/8mA	1'b1	YES	YES	1: PCMCIA_D_bit7,<I/O>,<HS> 9: TPO_data_bit3_pad,<O>,<HS> A: HIF_Data_bit7,<I/O> F: MIS_GPIO_bit91,<I/O> def: MIS_GPIO_bit91,<I/O>	gpio_91_ps
GPIO_92_TP 1_D7	AG2 5	4mA/8mA	1'b1	YES	YES	1: TP1_Data_bit7,<I>,<HS> A: HIF_Data_bit8,<I/O> F: MIS_GPIO_bit92,<I/O> def: MIS_GPIO_bit92,<I/O>	gpio_92_ps

GPIO_93_PC _CE1_1_N	AH2 5	4mA/8mA	1'b1	YES	YES	1: PCMCIA_CE0_0,<O>,<HS> A: HIF_Data_bit9,<I/O> F: MIS_GPIO_bit93,<I/O> def: MIS_GPIO_bit93,<I/O>	gpio_93_ps
GPIO_94_PC _A10	AG2 6	4mA/8mA	1'b1	YES	YES	1: PCMCIA_ADDR_bit10,<OD>,<HS> 9: TPO_data_bit4_pad,<O>,<HS> A: HIF_Data_bit10,<I/O> F: MIS_GPIO_bit94,<I/O> def: MIS_GPIO_bit94,<I/O>	gpio_94_ps
GPIO_95_PC _OE_N	AH2 6	X	1'b1	YES	YES	1: PCMCIA_OE_N,<O>,<HS> A: HIF_Data_bit11,<I/O> F: MIS_GPIO_bit95,<I/O> def: MIS_GPIO_bit95,<I/O>	gpio_95_ps
GPIO_96_PC _IORD_N	AJ2 6	X	1'b1	YES	YES	1: PCMCIA_IORD_N,<O>,<HS> A: HIF_Data_bit12,<I/O> F: MIS_GPIO_bit96,<I/O> def: MIS_GPIO_bit96,<I/O>	gpio_96_ps
GPIO_97_PC _A11	AG2 7	X	1'b1	YES	YES	1: PCMCIA_ADDR_bit11,<OD>,<HS> 9: TPO_data_bit5_pad,<O>,<HS> A: HIF_Data_bit13,<I/O> F: MIS_GPIO_bit97,<I/O> def: MIS_GPIO_bit97,<I/O>	gpio_97_ps
GPIO_98_PC _IOWR_N	AH2 7	X	1'b1	YES	YES	1: PCMCIA_IOWR_N,<O>,<HS> A: HIF_Data_bit14,<I/O> F: MIS_GPIO_bit98,<I/O> def: MIS_GPIO_bit98,<I/O>	gpio_98_ps
GPIO_99_PC _A9	AG2 8	4mA/8mA	1'b1	YES	YES	1: PCMCIA_ADDR_bit9,<OD>,<HS> 9: TPO_data_bit6_pad,<O>,<HS> A: HIF_Data_bit15,<I/O> F: MIS_GPIO_bit99,<I/O> def: MIS_GPIO_bit99,<I/O>	gpio_99_ps
GPIO_100_T PO_SYNC	AH2 8	4mA/8mA	1'b1	YES	YES	1: TPO_sync_pad,<O>,<HS> F: MIS_GPIO_bit100,<I/O> def: MIS_GPIO_bit100,<I/O>	gpio_100_ps
GPIO_101_P	AJ2	4mA/8mA	1'b1	YES	YES	1: PCMCIA_ADDR_bit8,<OD>,<HS>	gpio_101_ps

C_A8	8					> 9: TPO_data_bit7_pad,<O>,<HS> F: MIS_GPIO_bit101,<I/O> def: MIS_GPIO_bit101,<I/O>	
GPIO_102_T PO_D0	AJ2 9	4mA/8mA	1'b1	YES	YES	1: TPO_data_bit0_pad,<O>,<HS> 2: SPI_DI,<I/O>,<HS> E: test_en_bit11,<I/O> F: MIS_GPIO_bit102,<I/O> def: MIS_GPIO_bit102,<I/O>	gpio_102_p s
GPIO_103_P C_A13	AM3 1	4mA/8mA	1'b1	YES	YES	0: PCMCIA_CD1_N,<I>,<HS> 1: PCMCIA_ADDR_bit13,<OD>,<HS> 2: SPI_HOLD,<I/O>,<HS> 3: EJTAG_TRST_src0,<I> E: test_en_bit12,<I/O> F: MIS_GPIO_bit103,<I/O> def: MIS_GPIO_bit103,<I/O>	gpio_103_p s
GPIO_104_T PO_D1	AL3 1	4mA/8mA	1'b1	YES	YES	1: TPO_data_bit1_pad,<O>,<HS> 2: SPI_SCLK,<O>,<HS> E: test_en_bit13,<I/O> F: MIS_GPIO_bit104,<I/O> def: MIS_GPIO_bit104,<I/O>	gpio_104_p s
GPIO_105_P C_A14	AL3 2	4mA/8mA	1'b1	YES	YES	0: PCMCIA_CE0_1,<O>,<HS> 1: PCMCIA_ADDR_bit14,<OD>,<HS> 2: SPI_WP,<I/O>,<HS> 3: EJTAG_TDI_src0,<I> E: test_en_bit14,<I/O> F: MIS_GPIO_bit105,<I/O> def: MIS_GPIO_bit105,<I/O>	gpio_105_p s
GPIO_106_T PO_D2	AK3 1	4mA/8mA	1'b1	YES	YES	1: TPO_data_bit2_pad,<O>,<HS> 2: SPI_DO,<I/O>,<HS> E: test_en_bit15,<I/O> F: MIS_GPIO_bit106,<I/O> def: MIS_GPIO_bit106,<I/O>	gpio_106_p s
GPIO_107_P C_WE_N	AK3 2	4mA/8mA	1'b1	YES	YES	1: PCMCIA_WE_N,<O>,<HS> 2: SPI_CS_N,<O>,<HS> E: test_en_bit16,<I/O> F: MIS_GPIO_bit107,<I/O> def: MIS_GPIO_bit107,<I/O>	gpio_107_p s
GPIO_108_T PO_D3	AJ3 0	4mA/8mA	1'b1	YES	YES	1: TPO_data_bit3_pad,<O>,<HS> E: test_en_bit17,<I/O> F: MIS_GPIO_bit108,<I/O> def: MIS_GPIO_bit108,<I/O>	gpio_108_p s
GPIO_109_T PO_D4	AJ3 1	4mA/8mA	1'b1	YES	YES	1: TPO_data_bit4_pad,<O>,<HS> E: test_en_bit18,<I/O> F: MIS_GPIO_bit109,<I/O> def: MIS_GPIO_bit109,<I/O>	gpio_109_p s
GPIO_110_T PO_VAL	AJ3 2	4mA/8mA	1'b1	YES	YES	1: TPO_val_pad,<O>,<HS> E: test_en_bit19,<I/O> F: MIS_GPIO_bit110,<I/O> def: MIS_GPIO_bit110,<I/O>	gpio_110_p s

GPIO_111_T PO_D5	AH2 9	4mA/8mA	1'b1	YES	YES	1: TPO_data_bit5_pad,<O>,<HS> E: test_en_bit20,<I/O> F: MIS_GPIO_bit111,<I/O> def: MIS_GPIO_bit111,<I/O>	gpio_111_p s
GPIO_112_T PO_CLK	AH3 0	4mA/8mA	1'b1	YES	YES	1: TPO_clk_pad,<O>,<HS> E: test_en_bit21,<I/O> F: MIS_GPIO_bit112,<I/O> def: MIS_GPIO_bit112,<I/O>	gpio_112_p s
GPIO_113_T PO_D6	AH3 1	4mA/8mA	1'b1	YES	YES	1: TPO_data_bit6_pad,<O>,<HS> E: test_en_bit22,<I/O> F: MIS_GPIO_bit113,<I/O> def: MIS_GPIO_bit113,<I/O>	gpio_113_p s
GPIO_114_P C_A12	AH3 2	4mA/8mA	1'b1	YES	YES	0: PCMCIA_WAIT1_N,<I> 1: PCMCIA_ADDR_bit12,<OD>,<HS> 3: EJTAG_TDO,<O> E: test_en_bit23,<I/O> F: MIS_GPIO_bit114,<I/O> def: MIS_GPIO_bit114,<I/O>	gpio_114_p s
GPIO_115_T PO_D7	AG2 9	4mA/8mA	1'b1	YES	YES	1: TPO_data_bit7_pad,<O>,<HS> E: test_en_bit24,<I/O> F: MIS_GPIO_bit115,<I/O> def: MIS_GPIO_bit115,<I/O>	gpio_115_p s
GPIO_116_P C_A7	AG3 0	X	1'b1	YES	YES	1: PCMCIA_ADDR_bit7,<OD>,<HS> E: test_en_bit25,<I/O> F: MIS_GPIO_bit116,<I/O> def: MIS_GPIO_bit116,<I/O>	gpio_116_p s
GPIO_117_T P1_CLK	AG3 1	X	1'b1	YES	YES	1: TP1_CLK,<I>,<HS>,<AND> E: test_en_bit26,<I/O> F: MIS_GPIO_bit117,<I/O> def: MIS_GPIO_bit117,<I/O>	gpio_117_p s
GPIO_118_P C_A6	AG3 2	X	1'b1	YES	YES	1: PCMCIA_ADDR_bit6,<OD>,<HS> E: test_en_bit27,<I/O> F: MIS_GPIO_bit118,<I/O> def: MIS_GPIO_bit118,<I/O>	gpio_118_p s
GPIO_119_P C_RST	AF2 9	X	1'b1	YES	YES	1: PCMCIA_RST0,<OD>,<HS> E: test_en_bit28,<I/O> F: MIS_GPIO_bit119,<I/O> def: MIS_GPIO_bit119,<I/O>	gpio_119_p s
GPIO_120_P C_A5	AF3 0	4mA/8mA	1'b1	YES	YES	1: PCMCIA_ADDR_bit5,<OD>,<HS> E: test_en_bit29,<I/O> F: MIS_GPIO_bit120,<I/O> def: MIS_GPIO_bit120,<I/O>	gpio_120_p s
GPIO_121_P C_WAIT_N	AF3 1	4mA/8mA	1'b1	YES	YES	1: PCMCIA_WAIT0_N,<I> E: test_en_bit30,<I/O> F: MIS_GPIO_bit121,<I/O> def: MIS_GPIO_bit121,<I/O>	gpio_121_p s
GPIO_122_P C_A4	AF3 2	4mA/8mA	1'b1	YES	YES	1: PCMCIA_ADDR_bit4,<OD>,<HS> >	gpio_122_p s

						E: test_en_bit31,<I/O> F: MIS_GPIO_bit122,<I/O> def: MIS_GPIO_bit122,<I/O>	
GPIO_123_P C_INPACK_N	AE2 8	4mA/8mA	1'b1	YES	YES	0: PCMCIA_RST1,<OD>,<HS> 1: PCMCIA_INPACK0_N,<I>,<HS> 3: EJTAG_TMS_src0,<I> E: test_en_bit32,<I/O> F: MIS_GPIO_bit123,<I/O> def: MIS_GPIO_bit123,<I/O>	gpio_123_p s
GPIO_124_P C_A3	AE2 9	4mA/8mA	1'b1	YES	YES	1: PCMCIA_ADDR_bit3,<OD>,<HS> E: test_en_bit33,<I/O> F: MIS_GPIO_bit124,<I/O> def: MIS_GPIO_bit124,<I/O>	gpio_124_p s
GPIO_125_P C_REG_N	AD2 8	4mA/8mA	1'b1	YES	YES	0: PCMCIA_IREQ1_N,<I>,<HS> 1: PCMCIA_REG_N,<O> 3: EJTAG_TCLK_CLK_src0,<I>,<A ND> E: test_en_bit34,<I/O> F: MIS_GPIO_bit125,<I/O> def: MIS_GPIO_bit125,<I/O>	gpio_125_p s
GPIO_126_P C_A2	AD2 9	4mA/8mA	1'b1	YES	YES	1: PCMCIA_ADDR_bit2,<OD>,<HS> E: test_en_bit35,<I/O> F: MIS_GPIO_bit126,<I/O> def: MIS_GPIO_bit126,<I/O>	gpio_126_p s
GPIO_127_T P1_VAL	AC2 8	4mA/8mA	1'b1	YES	YES	1: TP1_VAL,<I>,<HS> 2: SD_CD_src1,<I>,<HS> E: test_en_bit36,<I/O> F: MIS_GPIO_bit127,<I/O> def: MIS_GPIO_bit127,<I/O>	gpio_127_p s
GPIO_128_P C_A1	AC2 9	4mA/8mA	1'b1	YES	YES	1: PCMCIA_ADDR_bit1,<OD>,<HS> 2: SD_WP_src1,<I>,<HS> E: test_en_bit37,<I/O> F: MIS_GPIO_bit128,<I/O> def: MIS_GPIO_bit128,<I/O>	gpio_128_p s
GPIO_129_T P1_SYC	AB2 8	4mA/8mA	1'b1	YES	YES	1: TP1_SYNC,<I>,<HS> 2: SD_CLK,<O>,<HS> E: test_en_bit38,<I/O> F: MIS_GPIO_bit129,<I/O> def: MIS_GPIO_bit129,<I/O>	gpio_129_p s
GPIO_130_P C_A0	AB2 9	4mA/8mA	1'b1	YES	YES	1: PCMCIA_ADDR_bit0,<OD>,<HS> 2: SD_CMD_src1,<I/O>,<HS> E: test_en_bit39,<I/O> F: MIS_GPIO_bit130,<I/O> def: MIS_GPIO_bit130,<I/O>	gpio_130_p s
GPIO_131_T P1_D0	AA2 8	4mA/8mA	1'b1	YES	YES	1: TP1_Data_bit0,<I>,<HS> 2: SD_Data2_src1,<I/O>,<HS> E: test_en_bit40,<I/O> F: MIS_GPIO_bit131,<I/O> def: MIS_GPIO_bit131,<I/O>	gpio_131_p s

GPIO_132_P C_D0	AA2 9	4mA/8m A	1'b1	YES	YES	1: PCMCIA_D_bit0,<I/O>,<HS> 2: SD_Data1_src1,<I/O>,<HS> E: test_en_bit41,<I/O> F: MIS_GPIO_bit132,<I/O> def: MIS_GPIO_bit132,<I/O>	gpio_132_p s
GPIO_133_T P1_D1	Y28	4mA/8m A	1'b1	YES	YES	1: TP1_Data_bit1,<I>,<HS> 2: SD_Data3_src1,<I/O>,<HS> E: test_en_bit42,<I/O> F: MIS_GPIO_bit133,<I/O> def: MIS_GPIO_bit133,<I/O>	gpio_133_p s
GPIO_134_P C_D1	Y29	4mA/8m A	1'b1	YES	YES	1: PCMCIA_D_bit1,<I/O>,<HS> 2: SD_Data0_src1,<I/O>,<HS> E: test_en_bit43,<I/O> F: MIS_GPIO_bit134,<I/O> def: MIS_GPIO_bit134,<I/O>	gpio_134_p s
GPIO_135_T P1_D2	W28	4mA/8m A	1'b1	YES	YES	1: TP1_Data_bit2,<I>,<HS> E: test_en_bit44,<I/O> F: MIS_GPIO_bit135,<I/O> def: MIS_GPIO_bit135,<I/O>	gpio_135_p s
GPIO_136_P C_D2	W29	4mA/8m A	1'b1	YES	YES	1: PCMCIA_D_bit2,<I/O>,<HS> E: test_en_bit45,<I/O> F: MIS_GPIO_bit136,<I/O> def: MIS_GPIO_bit136,<I/O>	gpio_136_p s
TEST_04	AB2 7	4mA/8m A	1'b1	NO	NO	4: TCON_bit3,<O> 5: TCON_bit30,<O> B: I2C2_SDA_SRC1,<I/O> D: I2C4_SDA_SRC2,<I/O> E: test_en_bit46,<I/O> F: MIS_GPIO_bit137,<I/O> def: MIS_GPIO_bit137,<I/O>	gpio_137_p s
TEST_03	AA2 7	4mA/8m A	1'b1	NO	NO	4: TCON_bit4,<O> B: I2C2_SCL_SRC1,<I/O> D: I2C4_SCL_SRC2,<I/O> E: test_en_bit47,<I/O> F: MIS_GPIO_bit138,<I/O> def: MIS_GPIO_bit138,<I/O>	gpio_138_p s
TEST_02	Y27	4mA/8m A	1'b1	NO	NO	4: TCON_bit7,<O> 9: ETN_LED_TXRX,<O> A: IRTX,<O> E: test_en_bit48,<I/O> F: MIS_GPIO_bit139,<I/O> def: MIS_GPIO_bit139,<I/O>	gpio_139_p s
TEST_01	W27	4mA/8m A	1'b1	NO	NO	4: TCON_bit17,<O> 9: ETN_LED_LINK,<O> A: IRTX,<O> E: test_en_bit49,<I/O> F: MIS_GPIO_bit140,<I/O> def: MIS_GPIO_bit140,<I/O>	gpio_140_p s
EMMC_RST_ N	AE3 1	X	1'b1	NO	NO	0: emmc_rst_n,<O> def: emmc_rst_n,<O>	Emmc_tst_n _ps
EMMC_CLK	AD3 1	X	1'b1	NO	NO	0: emmc_clk,<O> def: emmc_clk,<O>	Emmc_clk_ ps
EMMC_CMD	AC3 1	X	1'b1	NO	NO	0: emmc_cmd,<I/O> def: emmc_cmd,<I/O>	Emmc_cmd _ps
EMMC_DS	AC3 2	X	1'b1	NO	NO	0: emmc_ds,<I> def: emmc_ds,<I>	Emmc_ds_p s

EMMC_D5	AB3 1	X	1'b1	NO	NO	0: emmc_data_bit5,<I/O> def: emmc_data_bit5,<I/O>	Emmc_d5_p s
EMMC_D3	AB3 2	X	1'b1	NO	NO	0: emmc_data_bit3,<I/O> def: emmc_data_bit3,<I/O>	Emmc_d3_p s
EMMC_D4	AA3 1	X	1'b1	NO	NO	0: emmc_data_bit4,<I/O> def: emmc_data_bit4,<I/O>	Emmc_d4_p s
EMMC_D0	AA3 2	X	1'b1	NO	NO	0: emmc_data_bit0,<I/O> def: emmc_data_bit0,<I/O>	Emmc_d0_p s
EMMC_D1	Y31	X	1'b1	NO	NO	0: emmc_data_bit1,<I/O> def: emmc_data_bit1,<I/O>	Emmc_d1_p s
EMMC_D2	Y32	X	1'b1	NO	NO	0: emmc_data_bit2,<I/O> def: emmc_data_bit2,<I/O>	Emmc_d2_p s
EMMC_D7	W31	X	1'b1	NO	NO	0: emmc_data_bit7,<I/O> def: emmc_data_bit7,<I/O>	Emmc_d7_p s
EMMC_D6	W32	X	1'b1	NO	NO	0: emmc_data_bit6,<I/O> def: emmc_data_bit6,<I/O>	Emmc_d6_p s

3.18 Special Application Notice for Memory circuit.

SPI / eMMC share Function

Pin No.	eMMC	SPI Flash
AJ23		SPI_HOLD
AK23		SPI_WP
AJ24		SPI_DI0
AK25		SPI_CS
AK24		SPI_SCLK
AJ25		SPI_DO0
AL8	EMMC_D0	
AM9	EMMC_D1	
AL9	EMMC_D2	
AL7	EMMC_D3	
AM8	EMMC_D4	
AM7	EMMC_D5	
AL10	EMMC_D6	
AM10	EMMC_D7	
AL5	EMMC_CLK	
AM6	EMMC_CMD	
AM5	EMMC_RST_N	
AL6	EMMC_DS	

4 Electrical Characteristic

4.1 Absolute Maximum Ratings

WARNING : Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Parameter		Min	Max	Units
IO Supply Voltage (D3V3)		-0.5	3.63	V
Core Supply Voltage (CORE1V0)		-0.5	1.1	V
SCPU Supply Voltage (CPU1V0)		-0.5	1.1	V
10/100M ETN Supply Voltage(GHD1V0)		-0.5	1.1	V
EMMC IO Supply Voltage(EMMC1V8)		-0.5	1.98	V
Analog Supply Voltage (1.0V)	LV1V0	-0.5	1.2	V
	HDRX1V0			
	GHA1V0			
	GHP1V0			
Analog Supply Voltage (3.3V)	STB3V3_1	-0.5	3.63	V
	STB3V3_2			
	A3V3			
	HDRX3V3			
Analog Supply Voltage(1.5V)	DDR_1V5	-0.5	1.7	V
	LV1V5	-0.5	1.7	V
Input Voltage (D3V3)		-0.5	3.63	V
Input Voltage (5V Tolerance I/O)		-0.5	5.5	V

4.2 Recommended Operating Conditions

Parameter		Min	Typical	Max	Units
IO Supply Voltage (D3V3)		3.13	3.3	3.53	V
10/100M ETN Supply Voltage(GHD1V0)		0.9	1.0	1.05	V
HDMI Supply Voltage(HDRX1V0)		0.95	1.0	1.05	V
EMMC IO Supply Voltage(EMMC1V8)		1.7	1.8	1.95	V
Analog Supply Voltage (1.0V)	LV1V0	0.9	1.0	1.05	V
	USB1V0				
	GHA1V0				
	GHP1V0				
Analog Supply Voltage (3.3V)	STB3V3_1	3.13	3.3	3.53	V
	STB3V3_2				
	A3V3				
	HDRX3V3				
Analog Supply Voltage(1.5V)	DDR_1V5	1.425	1.5	1.575	V
	LV1V5	Vby1	1.5	1.575	V
	EPI	1.14	1.2	1.26	V

Note: measure from SoC ball side

Core/CPU voltage of SoC ball side

Parameter		Min	Typical	Max	Units
Core Supply Voltage (CORE1V0) Normal mode	VID_H	0.97	1.0	1.03	V
	VID_L	0.93	0.96	0.99	V
SCPU Supply Voltage (CPU1V0) Normal mode	VID_H	1.0	1.03	1.05	V
	VID_L	0.96	0.99	1.02	V

4.3 Crystal Condition

Parameter	Min	Typ	Max	Units
Nominal Frequency (Fundamental Mode)	-	27	-	MHz
Crystal Frequency Tolerance @ 25°C	-30		30	ppm
Crystal Frequency Stability (-25°C ~ 80 °C)	-50		50	ppm
Load Capacitance (C _L)			20	pF
Equivalent Series Resistance (ESR)			40	Ω
Shunt Capacitance (C ₀)			7	pF
Main Chip Frequency Stability (-5°C ~ 70 °C)	-100		100	ppm

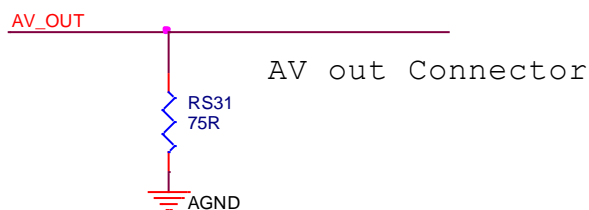
4.4 Analog Characteristics

Parameter		Min	Typ	Max	Units
CVBS input	DC-Characteristics, Note 1	-	-	-	V
	AC-Characteristics	0.2	1	1.6	(V _{p-p})V
CVBS output	DC-Characteristics, Note 2	-	0.5	-	V
	AC-Characteristics, Note 2	-	1.0	-	(V _{p-p})V
YPBPR input	DC-Characteristics, Note 1	-	-	-	V
	AC-Characteristics	0.8	1	1.3	(V _{p-p})V
VGA input	DC-Characteristics, Note 1	-	-	-	V
	AC-Characteristics	0.8	1	1.3	(V _{p-p})V
Audio input	DC-Characteristics, Note 1	-	-	1.65	V
	AC-Characteristics	-	-	1 (FSIV)	(rms)V
Audio output	DC-Characteristics, Note 1	-	1.65	-	V
	AC-Characteristics	-	-	0.95 (FSOV) (AOUT@10k Ohm loading 0.95 (FSOV) (HPOUT@32 Ohm loading,	(rms)V
Digital Inputs	V _{ih} , DC-Characteristics	2.0	-	-	V
	V _{il} , DC-Characteristics	-	-	0.8	V
Digital Outputs	V _{oh} , DC-Characteristics	2.4	-	-	V
	I _{oh}	4 or 8(Note3)			mA
	V _{ol} , DC-Characteristics	-	-	0.4	V
	I _{ol}	4 or 8(Note3)			mA

Note 1 : CVBS inputs, YPBPR inputs, VGA inputs and Audio inputs and outputs must be AC-coupled.

Note 2 : These parameters are based on following circuit.

Note 3: depend on pad register setting 4mA or 8mA.



4.5 Standby Power Consumption

4.6 Active Power Consumption

Parameter	Typical	Max	Units
CORE1V0	4.1	TBD	A
SCPU1V0	0.45	TBD	A
HDRX1V0 / LV1V0 /GHD1V0 / GHP1V0 / GHA1V0 (1.0V)	0.21	0.25	A
A3V3 / HDRX3V3 / STB3V3_1 / STB3V3_2 / RTC3V3/ D3V3 (3.3V)	0.315	0.33	A
EMMC_1V8 (1.8V)	0.1	0.15	A
DDR_1V5/LV1V5(including SIP KGD)	1.15	1.2	A
Power Dissipation	7.449	TBD	W

Note 1. Test condition: USB playback HEVC4K60Hz with Vby1 60Hz Panel.

Note 2. Typical value is under $T_j = 90^{\circ}\text{C}$, Max value is under $T_j = 125^{\circ}\text{C}$

Note 3. Not 100% tested.

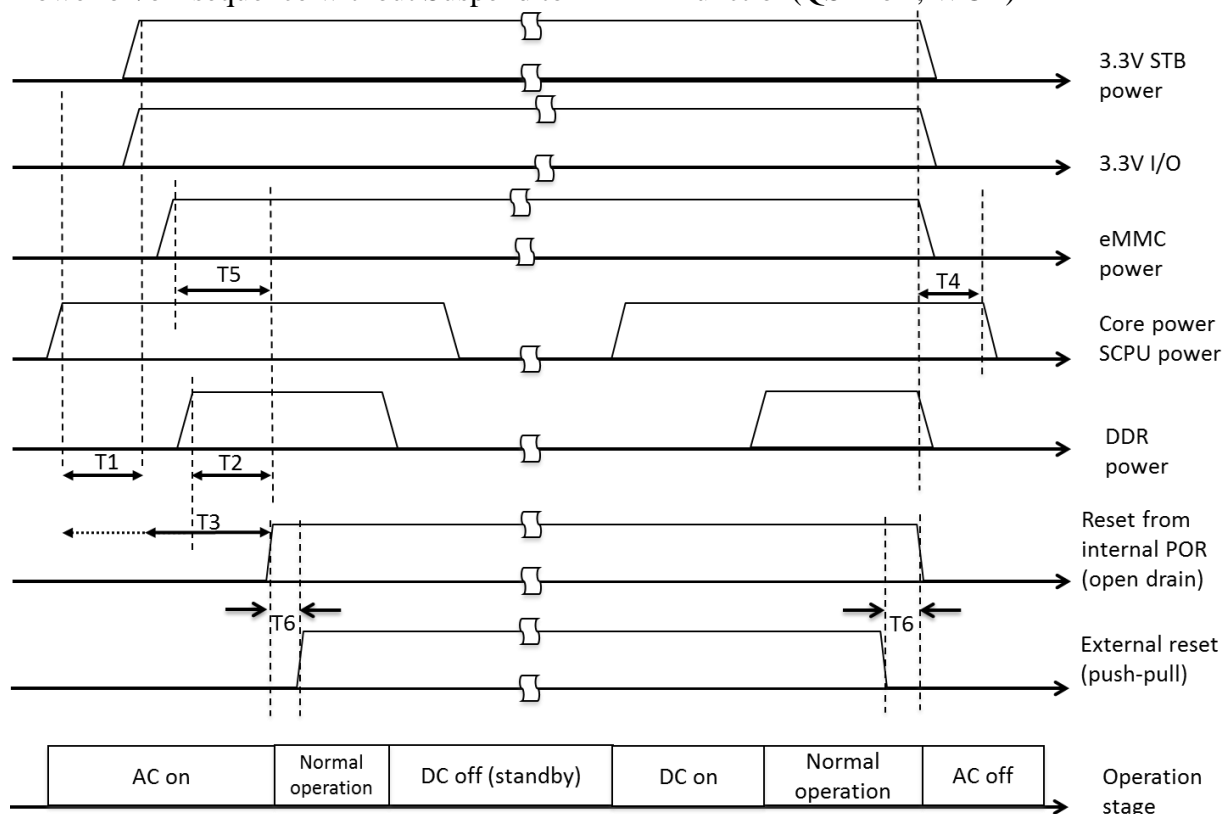
4.7 Thermal Condition

Symbol	Parameter	Value	Unit
T_s	Storage Temperature	-40~150	$^{\circ}\text{C}$
T_a	Ambient temperature	60	$^{\circ}\text{C}$
$T_j \text{ max}$	Max junction temperature	125	$^{\circ}\text{C}$
$T_c \text{ max}$	Max case temperature	100	$^{\circ}\text{C}$
θ_{ja}	Junction to ambient thermal resistance	6.18	$^{\circ}\text{C}/\text{W}$
Max. PD	Maximum Power Dissipation	10.08	W
PCB conditions	PCB Dimensions	185 x 215 x 1.6 mm ^{^3}	
	Number of Cu layer PCB	4-layer PCB	
Heat Sink	Size	35x35x15 mm ^{^3}	

4.8 Power On/Off Sequence

RTD28xx supports suspend to DRAM function. The description shows below the power on/off sequence w/wo suspend to DRAM function.

4.8.1 Power on/off sequence without Suspend to DRAM Function(QSM off, WOL)

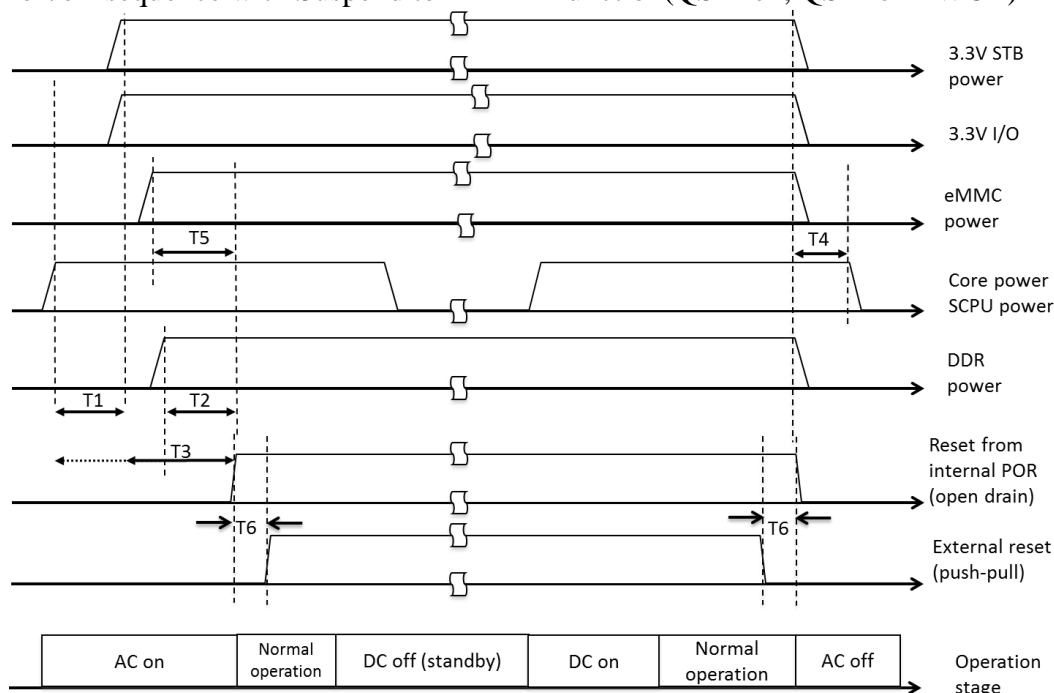


Parameter	Value			Unit
	Min	Typ	Max	
T1	-250		250	ms
T2	1			ms
T3	130		170	ms
T4	> 0			ms
T5	1			ms
T6	>=0			ms

Note:

1. T1: Doesn't care power on sequence on Core power, 3.3V IO and 3.3V STB power.
2. T2: DDR stable power supply before chip H/W reset signal go high (release chip H/W reset).
3. T3: T3 is the interval time for chip H/W reset. It is from the latest stable power (Core power, 3.3V IO and 3.3V STB) to chip H/W reset signal go high (release chip H/W reset).
4. T4: Core power and SCPU power need to keep minimum operating voltage before internal or external H/W reset signal go low
5. T5: eMMC stable power supply before chip H/W reset signal go high (release chip H/W reset).
6. T6: To prevent voltage conflict of internal and external reset, T6 should be >=0.

4.8.2 Power on/off sequence with Suspend to DRAM Function(QSM on, QSM on +WOL)

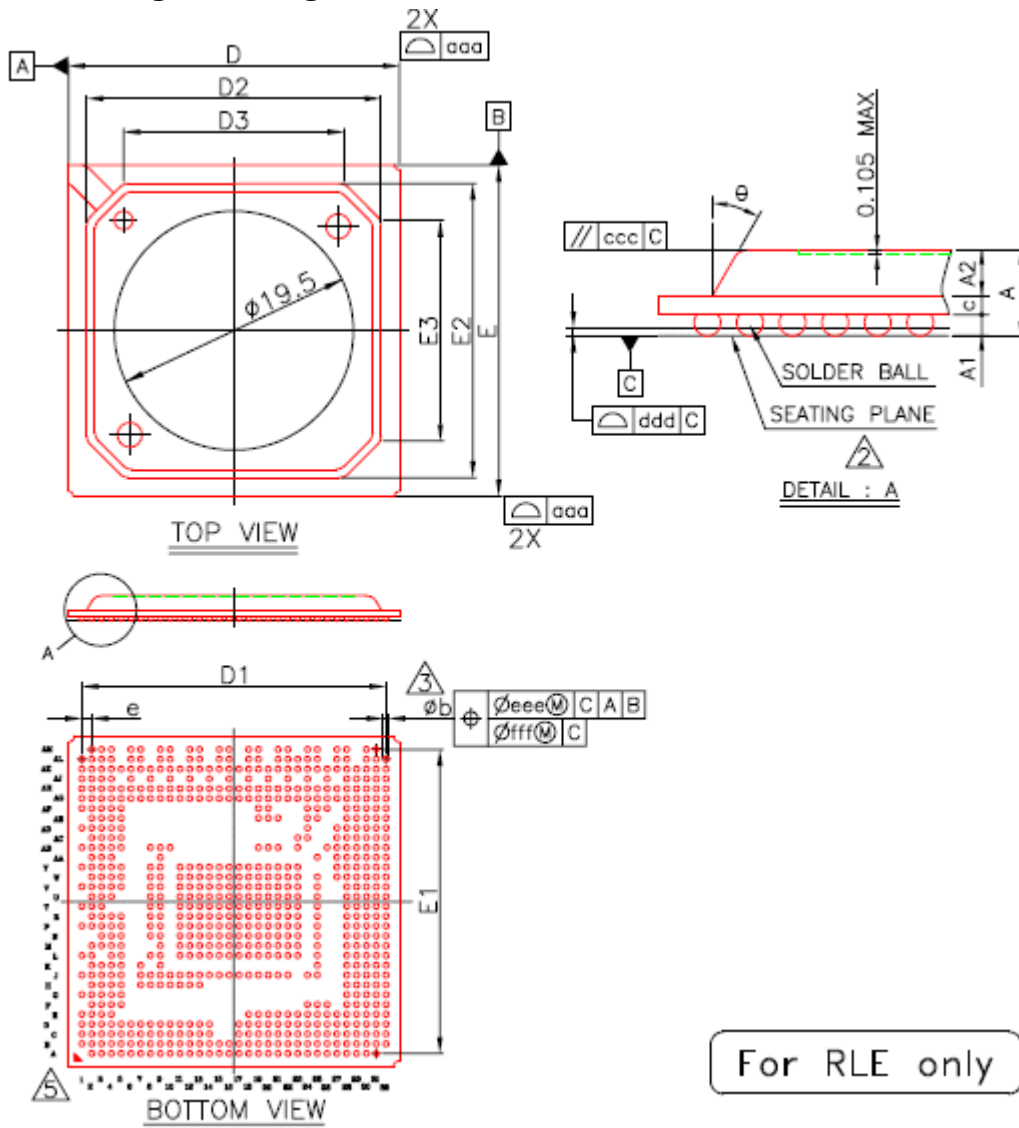


Parameter	Value			Unit
	Min	Typ	Max	
T1	-250		250	ms
T2	1			ms
T3	130		170	ms
T4	> 0			ms
T5	1			ms
T6	>=0			ms

- Note:
1. T1: Doesn't care power on sequence on Core power, 3.3V IO and 3.3V STB power.
 2. T2: DDR stable power supply before chip H/W reset signal go high (release chip H/W reset).
 3. T3: T3 is the interval time for chip H/W reset. It is from the latest stable power (Core power, 3.3V IO and 3.3V STB) to chip H/W reset signal go high (release chip H/W reset).
 4. T4: Core power and SCPU power need to keep minimum operating voltage before internal or external H/W reset signal go low
 5. T5: eMMC stable power supply before chip H/W reset signal go high (release chip H/W reset).
 6. DDR power always on for suspend to DRAM function.
 7. T6: To prevent voltage conflict of internal and external reset, T6 should be >=0.

5 Package Drawing

5.1 Package Drawing



5.2 Package Dimension Specification

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.99	2.08	2.17	0.078	0.082	0.085
A1	0.30	0.35	0.40	0.012	0.014	0.016
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	0.40	0.45	0.50	0.016	0.018	0.020
c	0.51	0.56	0.61	0.020	0.022	0.024
D	26.80	27.00	27.20	1.055	1.063	1.071
D1	----	24.80	----	----	0.976	----
D2	23.80	24.00	24.20	0.937	0.945	0.953
D3	----	18.00	----	----	0.709	----
E	26.80	27.00	27.20	1.055	1.063	1.071
E1	----	24.80	----	----	0.976	----
E2	23.80	24.00	24.20	0.937	0.945	0.953
E3	----	18.00	----	----	0.709	----
e	----	0.80	----	----	0.031	----
aaa	0.15			0.006		
ccc	0.20			0.008		
ddd	0.20			0.008		
eee	0.15			0.006		
fff	0.08			0.003		
θ	30° TYP			30° TYP		

NOTE:

1. CONTROLLING DIMENSION: MILLIMETER.

△ PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

△ DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. SPECIAL CHARACTERISTICS C CLASS: ccc , ddd

△ THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

6. REFERENCE DOCUMENT : JEDEC PUBLICATION 95
DESIGN GUIDE 4.5